e·MMC™ Memory

MTFC4GACAAAM-1M WT
MTFC8GACAAAM-1M WT
MTFC16GAAAADV-2M WT

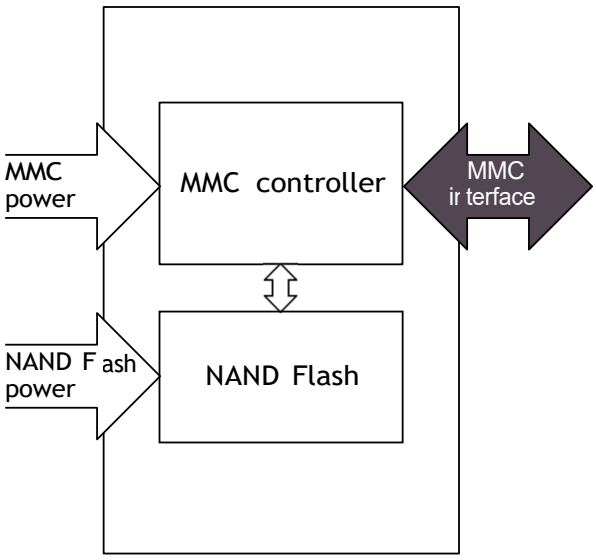
Features

- MultiMediaCard (MMC) controller and NAND Flash
- 153-ball VFBGA and 169-ball VFBGA (RoHS compliant, "green package")
- V_{CC}: 2.7–3.6V
- V_{CCQ} (dual voltage): 1.65–1.95V; 2.7–3.6V
- Temperature ranges
  - Operating temperature: –25°C to +85°C
  - Storage temperature: –40°C to +85°C

MMC-Specific Features

- JEDEC/MMC standard version 4.51-compliant (JEDEC Standard No. 84-B451) – SPI mode not supported 1
  - Advanced 11-signal interface
  - x1, x4, and x8 I/Os, selectable by host
  - SDR/DDR modes up to 52 MHz clock speed
  - HS200 mode
  - Real-time clock
  - Command classes: class 0 (basic); class 2 (block read); class 4 (block write); class 5 (erase); class 6 (write protection); class 7 (lock card)
  - Temporary write protection
  - Boot operation (high-speed boot)
  - Sleep mode
  - Replay-protected memory block (RPMB)
  - Secure erase and secure trim
  - Hardware reset signal
  - Multiple partitions with enhanced attribute
  - Permanent and power-on write protection
  - High-priority interrupt (HPI)

Figure 1: Micron *e*·MMC Device



MMC-Specific Features (Continued)

- Background operation
- Reliable write
- Discard and sanitize
- Extended partitioning
- Context ID
- Data TAG
- Packed commands
- Dynamic device capacity
- Backward compatible with previous MMC
- Thermal specification
- Cache

- ECC and block management implemented

Note: 1. The JEDEC specification is available at /default/files/docs/JESD84-B451.pdf.

e·MMC Performance and Current Consumption

Table 1: MLC Partition Performance

Condition [1]	Typical Values			Unit
	4GB	8GB	16GB	
Sequential Write	11	24	24	MB/s
Sequential Read	80	120	120	MB/s
Random Write	1000	1000	1000	IOPS
Random Read	4000	4000	4000	IOPS

Note: 1. Bus in x8 I/O and HS200 modes. Sequential access of 1MB chunk; random access of 4KB chunk over 1GB span. Additional performance data, such as system performance on a specific application board, will be provided in a separate document upon customer request.

Table 2: 52 MHz DDR2 Performance

Condition [1]	Typical Values			Unit
	4GB	8GB	16GB	
Sequential Write	11	24	24	MB/s
Sequential Read	75	80	80	MB/s
Random Write	1000	1000	1000	IOPS
Random Read	3800	3800	3800	IOPS

Note: 1. Bus in x8 I/O and 52 MHz DDR2 modes. Sequential access of 1MB chunk; random access of 4KB chunk over 1GB span. Additional performance data, such as system performance on a specific application board, will be provided in a separate document upon customer request.

Table 3: Current Consumption

Condition [1]	Typical Values (I_{CC}/I_{CCQ})			Unit
	4GB	8GB	16GB	
Write	50/20	60/20	60/20	mA
Read	60/60	60/60	60/60	mA
Sleep	0/180	0/180	0/180	uA
Auto-Standby	25/150	50/180	50/180	uA

Note: 1. Bus in x8 I/O and HS200 modes. V_{CC} = 3.6V and V_{CCQ} = 1.95V. 25°C. Measurements done as average RMS current consumption. I_{CCQ} in READ operation might be affected by tester load.

Part Numbering Information

Micron®*e*·MMC memory devices are available in different configurations and densities.

Figure 2: *e*·MMC Part Numbering

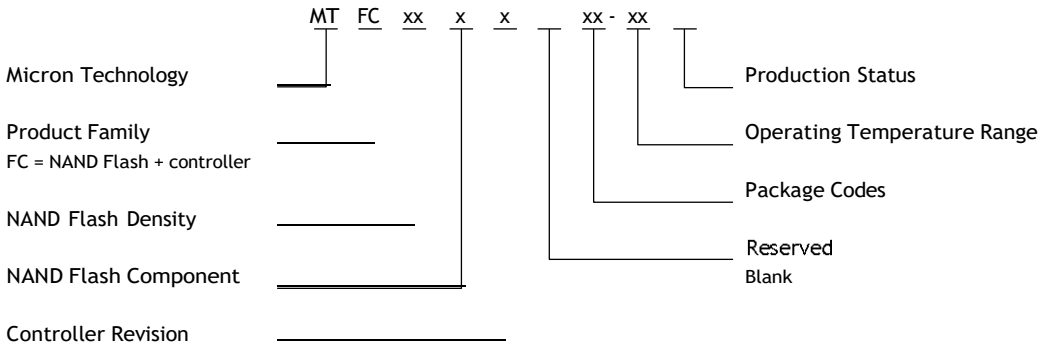


Table 4: Ordering Information

Base Part Number	Density	Package	Shipping
MTFC4GACAAAM-1M WT	4GB	153-ball VFBGA 11.5mm x 13.0mm x 1.0mm	Tray Tape and reel
MTFC8GACAAAM-1M WT	8GB	153-ball VFBGA 11.5mm x 13.0mm x 1.0mm	Tray Tape and reel
MTFC16GAAAADV-2M WT	16GB	169-ball VFBGA 12.0mm x 16.0mm x 1.0mm	Tray Tape and reel

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: der.

General Description

Micron *e*·MMC is a communication and mass data storage device that includes a MultiMediaCard (MMC) interface, a NAND Flash component, and a controller on an advanced 11-signal bus, which is compliant with the MMC system specification. Its low cost, small size, Flash technology independence, and high data throughput make *e*·MMC ideal for smartphones, digital cameras, PDAs, MP3s, and other portable applications.

The nonvolatile *e*·MMC draws no power to maintain stored data, delivers high performance across a wide range of operating temperatures, and resists shock and vibration disruption.

Signal Descriptions

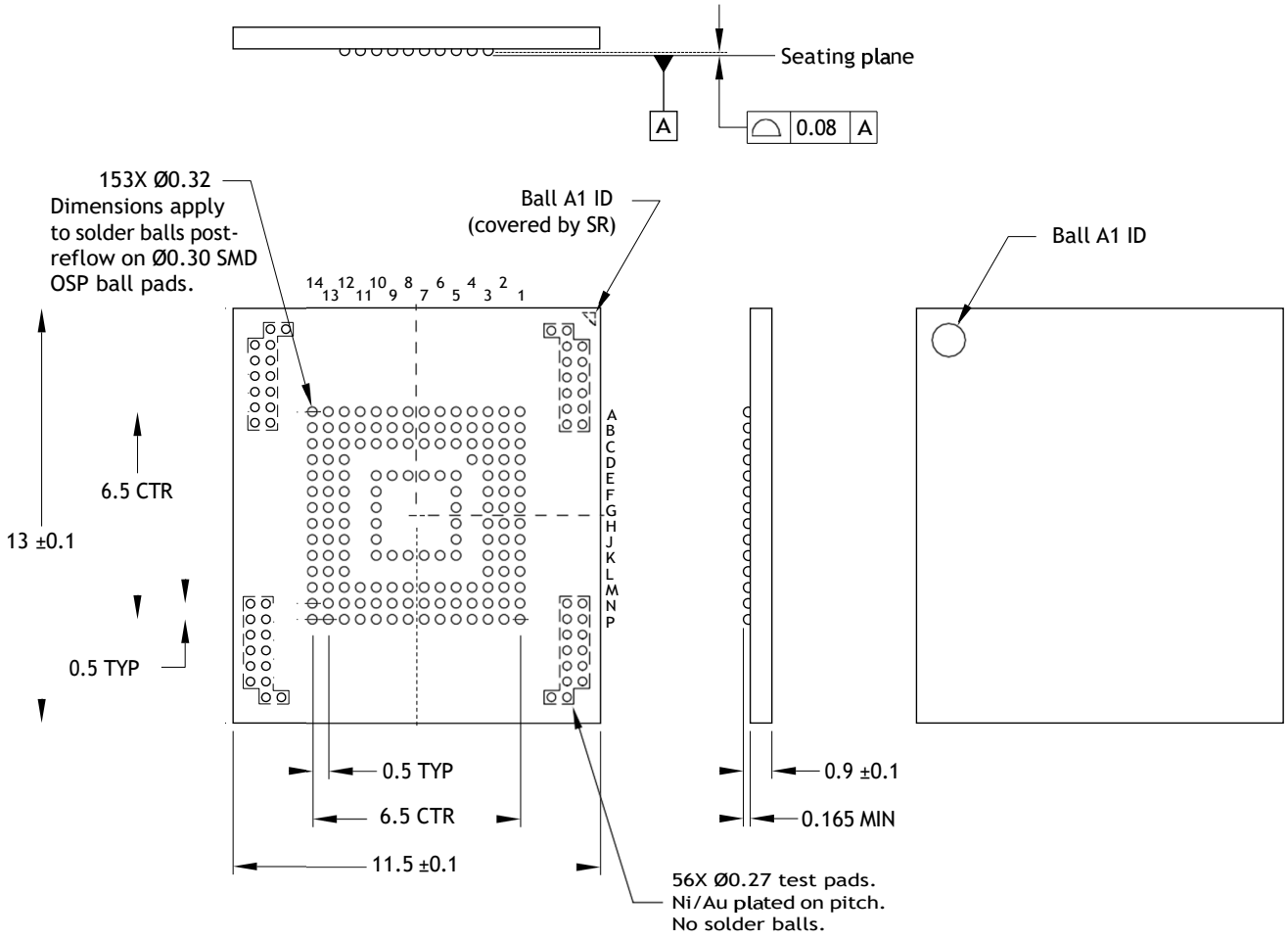
Table 5: Signal Descriptions

Symbol	Type	Description
CLK	Input	Clock: Each cycle of the clock directs a transfer on the command line and on the data line(s). The frequency can vary between the minimum and the maximum clock frequency.
RST_n	Input	Reset: The RST_n signal is used by the host for resetting the device, moving the device to the pre-idle state. By default, the RST_n signal is temporarily disabled in the device. The host must set ECSD register byte 162, bits[1:0] to 0x1 to enable this functionality before the host can use it.
CMD	I/O	Command: This signal is a bidirectional command channel used for command and response transfers. The CMD signal has two bus modes: open-drain mode and push-pull mode (see Operating Modes). Commands are sent from the MMC host to the device, and responses are sent from the device to the host.
DAT[7:0]	I/O	Data I/O: These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-on or assertion of the RST_n signal, only DAT0 is used for data transfer. The MMC controller can configure a wider data bus for data transfer either using DAT[3:0] (4-bit mode) or DAT[7:0] (8-bit mode). *e*·MMC includes internal pull-up resistors for data lines DAT[7:1]. Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT[3:1] lines. Upon entering the 8-bit mode, the device disconnects the internal pull-ups on the DAT[7:1] lines.
V_{CC}	Supply	V_{CC}: NAND interface (I/F) I/O and NAND Flash power supply.
V_{CCQ}	Supply	V_{CCQ}: *e*·MMC controller core and *e*·MMC I/F I/O power supply.
V_{SS}[1]	Supply	V_{SS}: NAND I/F I/O and NAND Flash ground connection.
V_{SSQ}[1]	Supply	V_{SSQ}: *e*·MMC controller core and *e*·MMC I/F ground connection.
V_{DDIM}		Internal voltage node: At least a 0.1µF capacitor is required to connect V_{DDIM} to ground. A 1µF capacitor is recommended. Do not tie to supply voltage or ground.
NC	–	No connect: No internal connection is present.
RFU	–	Reserved for future use: No internal connection is present. Leave it floating externally.

Note: 1. V_{SS} and V_{SSQ} are connected internally.

Package Dimensions

Figure 3: 153-Ball VFBGA – 11.50mm x 13.00mm x 1.00mm (Package Code: AM)



Note: 1. Dimensions are in millimeters.