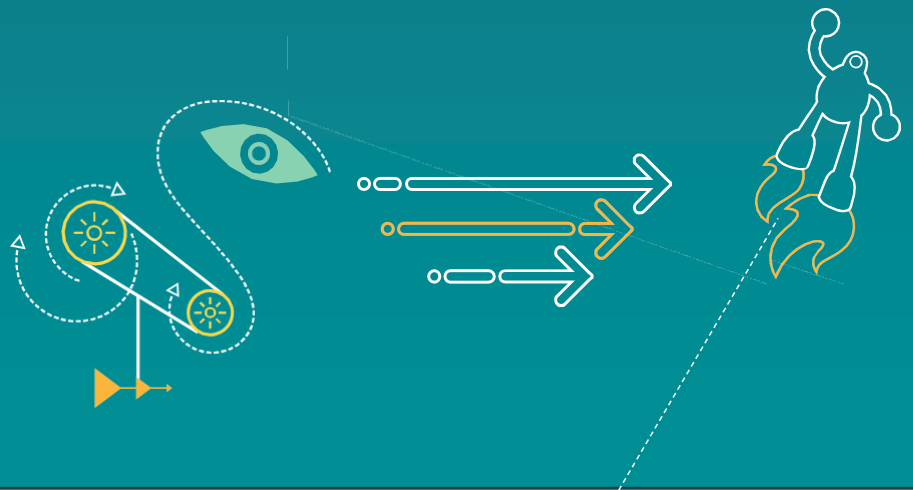
QCA402x
Hardware Design Guidelines

Qualcomm Technologies, Inc.

80-WL500-5 Rev. B



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Revision History

Revision	Date	Description
A	April 2017	Initial release
B	August 2017	Updated for CS feature

Contents

Section 1

QCA402x Introduction

Section 1.1

Overview

QCA402x – Hostless IoE Client Platform SoC

QCA4020 : M4 CPU + CNSS + Dual Band 802.11abgn WLAN
QCA4024 : M4 CPU + CNSS (15.4+BLE)

Features and packages:

- Dual Band 802.11 a/b/g/n Wi-Fi + Bluetooth Low Energy 5 + 802.15.4 connectivity (QCA4020)
- Bluetooth Low Energy 5 + 802.15.4 (QCA4024)
- A single regulated 3.3 V supply operation for QCA4020, QCA4024 (if VIO is 1.8 V, 1.8 VIO power supply required)
- Highly integrated WLAN SoC for 2.4/5G 802.11 abgn WLAN , BT LE and 802.15.4 technology
- Advanced Hardware-Based Security features in a low power, cost-optimized single-chip solution
- Support 20 MHz (and optionally 40 MHz) at 2.4 GHz and support 20/40 MHz at 5 GHz
- Support external PA for BLE and 802.15.4 with control logics
- Integrated Sensor Hub: for post-processing to enable the low power sensor use cases (1.8v IO only)

QCA4020/4024 Schedule	
CS	Sep 30, 2017

Parameter	Specification	
WLAN technology	802.11a/b/g/n with advanced features	
BT technology	BT Low Energy 5	
802.15.4 technology	802.15.4	
Best-in-class coexistence	Wi-Fi/BLE coexistence engine; BLE-802.15.4 coexistence	
Package	QCA 4020	▪ 217-ball MSP ▪ 11.2 mm×11.2 mm×0.876 mm ▪ 0.65 mm pitch
	QCA 4024	▪ 68-pin MQFN ▪ 8.0 mm×8.0 mm×0.85 mm ▪ 0.4 mm pitch
Interfaces (supporting low power)	▪ SPI, UART, PWM, I2S, I2C, SDIO, and ADC as well as GPIOs	
WLAN channel bandwidths	20/40 MHz	
WLAN TCIP/IP throughput	Hostless : > 20 Mbps	
WLAN maximum P_{OUT} (at the balun)	▪ Up to +19 dBm (11b, 2.4 GHz) ▪ Up to +19 dBm (OFDM, 2.4 GHz) ▪ Up to +16 dBm (OFDM, 5 GHz)	
BLE Rx sensitivity Tx output power (at chip output)	▪ -96 dBm GFSK ▪ +4 dBm	
15.4 Rx sensitivity Tx output power (at chip output)	▪ -103 dBm (1% PER) ▪ +4 dBm	
Power supply	Regulated 3.3 V, 1.8V (VIO if needs).	

QCA402x – Hostless IoE Client Platform SoC

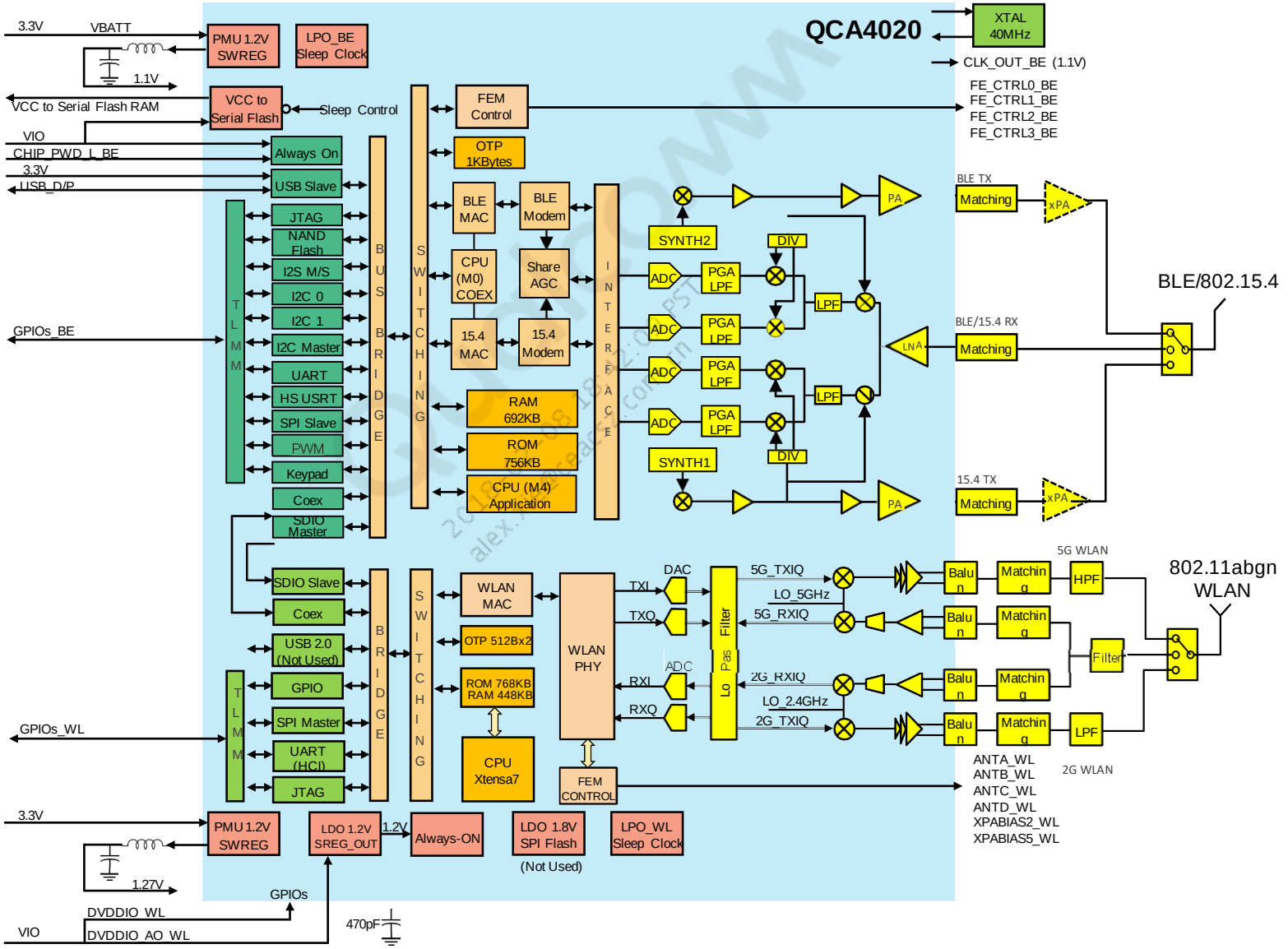
QCA4020 (M4 CPU + CNSS + WLAN)

1. **ARM Cortex-M4F Application Processor**
   - 128 MHz, 692 KB ROM/RAM
2. **CNSS (Connectivity Subsystem)**
   - BLE 4.2: Host and Controller
   - BT v5: 2 MbpsPHY, Adv length extensions
   - 802.15.4 - LMAC, PHY, encrypt/decrypt
3. **WLAN**
   - 1x1 dual-band 802.11abgn
   - Tensilica LX processor
   - STBC, TXBFee RX, Green TX, Low power listen, Fast RX antenna diversity.
4. **Co-existence**
   - Wi-Fi + BT + 802.15.4 Coex.
   - Co-existence with an external device vis PTA 3-wires master interface.
   - Antennas options vs co-existing (see next page).
5. **External QSPI serial Flash**
   - Low speed: 8 MHz at boot-up
   - High speed: Either 64 MHz or 96 MHz QSPI access.
6. **Host-less mode**
   - SPI Master or SDIO Slave interface with other Host
7. **PMU**
   - 1.8 V/3.3 V IO support. (1.8 V only for ES).
   - 1.1 V Buck converters for internal Digital/Analog
8. **Package**
   - 11.2x11.2 mm VFBGA217, 0.65 mm pitch for 4-layer PCB design.

QCA4024 (M4 CPU + CNSS)

1. **ARM Cortex-M4F Application Processor**
   - 128 MHz, 692 KB RAM.
2. **CNSS (Connectivity Subsystem)**
   - Cortex M0 connectivity processor
   - BLE 4.2: Host and Controller
   - BT v5: 2 MbpsPHY, Adv length extensions
   - IEEE802.15.4 v2006 with CSL feature
3. **Co-existence**
   - BT + 802.15.4 Coex.
   - Configurable Priority Assignment
   - Co-existence with an external device vis 3-wire PTA master/slave interface.
   - Antennas options vs co-existing (see next page).
4. **External QSPI serial Flash**
   - 8 MHz at boot-up
   - Either 64 MHz or 96 MHz 4-bits access.
5. **Host-less mode**
6. **PMU**
   - VBATT: 1.8 V ~ 3.6 V
   - 1.8 V/3.3 V IO support. (1.8 V only for ES).
   - 1.8 V LDO for IO voltage
   - 1.1 V Buck converter for internal Digital/Analog
7. **Package**
   - 8x8 mm, MQFN68, 0.4 mm pitch for either 2-layer or 4-layer PCB design.

QCA4020 Architecture



QCA4024 Architecture