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Read This First

This document describes the external interface (XINTF) used in the F2833x device. The XINTF is a nonmultiplexed asynchronous bus.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h or with a leading 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the related devices and related support tools. Copies of these documents are available on the Internet at *Tip:* Enter the literature number in the search box provided at

Data Manual—

SPRS439— TMS320F28335, F28334, F28332 Digital Signal Controllers (DSCs) Data Manual contains the pinout, signal descriptions, as well as electrical and timing specifications for the F2833x devices.

CPU User's Guides—

SPRU430— TMS320C28x DSP CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). It also describes emulation features available on these DSPs.

SPRUEO2— TMS320C28x Floating Point Unit and Instruction Set Reference Guide describes the floating-point unit and includes the instructions for the FPU.

Peripheral Guides—

SPRU566— TMS320x28xx, 28xxx Peripheral Reference Guide describes the peripheral reference guides of the 28x digital signal processors (DSPs).

SPRUFB0— TMS320x2833x System Control and Interrupts Reference Guide describes the various interrupts and system control features of the 2833x digital signal controllers (DSCs).

SPRU812— TMS320x2833x Analog-to-Digital Converter (ADC) Reference Guide describes how to configure and use the on-chip ADC module, which is a 12-bit pipelined ADC.

SPRU949— TMS320x2833x External Interface (XINTF) User's Guide describes the XINTF, which is a nonmultiplexed asynchronous bus, as it is used on the 2833x devices.

SPRU963— TMS320x2833x Boot ROM User's Guide describes the purpose and features of the bootloader (factory-programmed boot-loading software) and provides examples of code. It also describes other contents of the device on-chip boot ROM and identifies where all of the information is located within that memory.

SPRUFB7— TMS320x2833x Multichannel Buffered Serial Port (McBSP) User's Guide describes the McBSP available on the F2833x devices. The McBSPs allow direct interface between a DSP and other devices in a system.

SPRUFB8— TMS320x2833x Direct Memory Access (DMA) Reference Guide describes the DMA on the 2833x devices.

SPRU791— TMS320x28xx, 28xxx Enhanced Pulse Width Modulator (ePWM) Module Reference Guide describes the main areas of the enhanced pulse width modulator that include digital motor control, switch mode power supply control, UPS (uninterruptible power supplies), and other forms of power conversion.

SPRU924— TMS320x28xx, 28xxx High-Resolution Pulse Width Modulator (HRPWM) describes the operation of the high-resolution extension to the pulse width modulator (HRPWM).

SPRU807— TMS320x28xx, 28xxx Enhanced Capture (eCAP) Module Reference Guide describes the enhanced capture module. It includes the module description and registers.

SPRU790— TMS320x28xx, 28xxx Enhanced Quadrature Encoder Pulse (eQEP) Reference Guide describes the eQEP module, which is used for interfacing with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine in high performance motion and position control systems. It includes the module description and registers.

SPRU074— TMS320x28xx, 28xxx Enhanced Controller Area Network (eCAN) Reference Guide describes the eCAN that uses established protocol to communicate serially with other controllers in electrically noisy environments.

SPRU051— TMS320x28xx, 28xxx Serial Communication Interface (SCI) Reference Guide describes the SCI, which is a two-wire asynchronous serial port, commonly known as a UART. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format.

SPRU059— TMS320x28xx, 28xxx Serial Peripheral Interface (SPI) Reference Guide describes the SPI - a high-speed synchronous serial input/output (I/O) port - that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmed bit-transfer rate.

SPRU721— TMS320x28xx, 28xxx Inter-Integrated Circuit (I2C) Reference Guide describes the features and operation of the inter-integrated circuit (I2C) module that is available on the TMS320x280x digital signal processor (DSP).

Tools Guides—

SPRU513— TMS320C28x Assembly Language Tools User's Guide describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

SPRU514— TMS320C28x Optimizing C Compiler User's Guide describes the TMS320C28x™ C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

SPRU608— The TMS320C28x Instruction Set Simulator Technical Overview describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x™ core.

SPRU625— TMS320C28x DSP/BIOS Application Programming Interface (API) Reference Guide describes development using DSP/BIOS.

TMS320x2833x DSC External Interface (XINTF)

The external interface (XINTF) is a nonmultiplexed asynchronous bus, similar to the TMS320x281x external interface.

This guide is applicable for the XINTF found on the TMS320x2833x family of processors. This includes all Flash-based and RAM-based devices within the 2833x family.

1.1 Functional Description

The XINTF is mapped into three fixed memory-mapped zones as defined in Section 1.1.3.

Each of the 28x XINTF zones has a chip-select signal that is toggled when an access is made to that particular zone. On some devices the chip-select signals for two zones may be internally ANDed together to form a single shared chip select. In this manner, the same memory is connected to both zones or external decode logic can be used to separate the two.

Each of the three zones can also be programmed with a specified number of wait states, strobe signal set-up and hold timing. The number of wait states, set-up and hold timing is separately specified for a read access and a write access. In addition, each zone can be programmed for extending wait states externally using the XREADY signal or not. The programmable wait-state, chip-select and programmable strobe timing enables glueless interface to external memories and peripherals.

You specify the set-up/hold and access wait states for each XINTF zone by configuring the associated XTIMINGx registers. The access timing is based on an internal clock called XTIMCLK. XTIMCLK can be set to the same rate as the SYSCLKOUT or to one-half of SYSCLKOUT. The rate of XTIMCLK applies to all of the XINTF zones. XINTF bus cycles begin on the rising edge of XCLKOUT and all timings and events are generated with respect to the rising edge of XTIMCLK.

1.1.1 Differences from the TMS320x281x XINTF

The XINTF described in this document is very similar to the TMS320x281x XINTF. The main differences are:

- **Data Bus Width:**
  Each XINTF zone can be configured individually to use a 16-bit or 32-bit data bus. Using the 32-bit mode improves performance since 32 bits of data can be read or written in a single access. The data bus width does not change the size of the XINTF zones or memory reach. In 32-bit mode, the lowest address line XA0 becomes a 2nd write enable. The 281x XINTF is limited to a 16-bit data bus.
- **Address Bus Reach:**
  The address reach has been extended to 20 address lines. Zone 6 and Zone 7 both use the full address reach of 1M x 16 words each. The 281x address reach is 512k x 16 words.
- **Direct Memory Access (DMA):**
  All three XINTF zones are connected to the on-chip DMA module. The DMA can be used to copy code and data to or from the XINTF while the CPU is processing other data. The 281x devices do not include a DMA.

- **XINTF Clock Enable:**
  The XINTF clock (XTIMCLK) is disabled by default to save power. XTIMCLK can be enabled by writing a 1 to bit 12 of the PCLKCR3 register. PCLKCR3 is documented in the device-specific system control and interrupts user's guide. For the F2833x devices, it is *TMS320F2833x System Control and Interrupts Reference Guide* (literature number SPRUFB0). Turning off XTIMCLK does not turn off XCLKOUT. There is a separate control to turn off XCLKOUT. On the 281x, XTIMCLK is always enabled.
- **XINTF Pin MUXing:**
  Many of the XINTF pins are MUXed with general purpose I/O. The GPIO mux registers must be configured for XINTF operation before you can use the XINTF. On the 281x the XINTF has dedicated pins.
- **Number of Zones and Chip Select Signals:**
  The number of XINTF zones has been reduced to 3: Zone 0, Zone 6 and Zone 7. Each of these zones has a dedicated chip select signal. Zone 0 is still read-followed-by write protected as described in Section 1.1.4. On the 2812 devices, some zone chip-select signals are shared between zones. Zone 0 and Zone 1 share XZCS0AND1 and Zone 6 and Zone 7 share XZCS6AND7.
- **Zone 7 Memory Mapping:**
  Zone 7 is always mapped. On the 281x devices the MPNMC input signal determines if Zone 7 is mapped. Zone 6 and 7 do not share any locations. On 281x, Zone 7 is mirrored within Zone 6.
- **Zone Memory Map Locations:**
  Zone 0 starts at address 0x4000 and is 4K x 16. On 281x Zone 0 starts at address 0x2000 and is 8K x 16. Zone 6 and 7 are both 1M x 16 and start at 0x100000 and 0x200000 respectively. On 281x these two zones are 512K x 16 and 16K x 16.
- **EALLOW protection:**
  The XINTF registers are now EALLOW protected. On 281x the XINTF registers were not EALLOW protected.

For timing information refer to the latest data manual for your particular device.

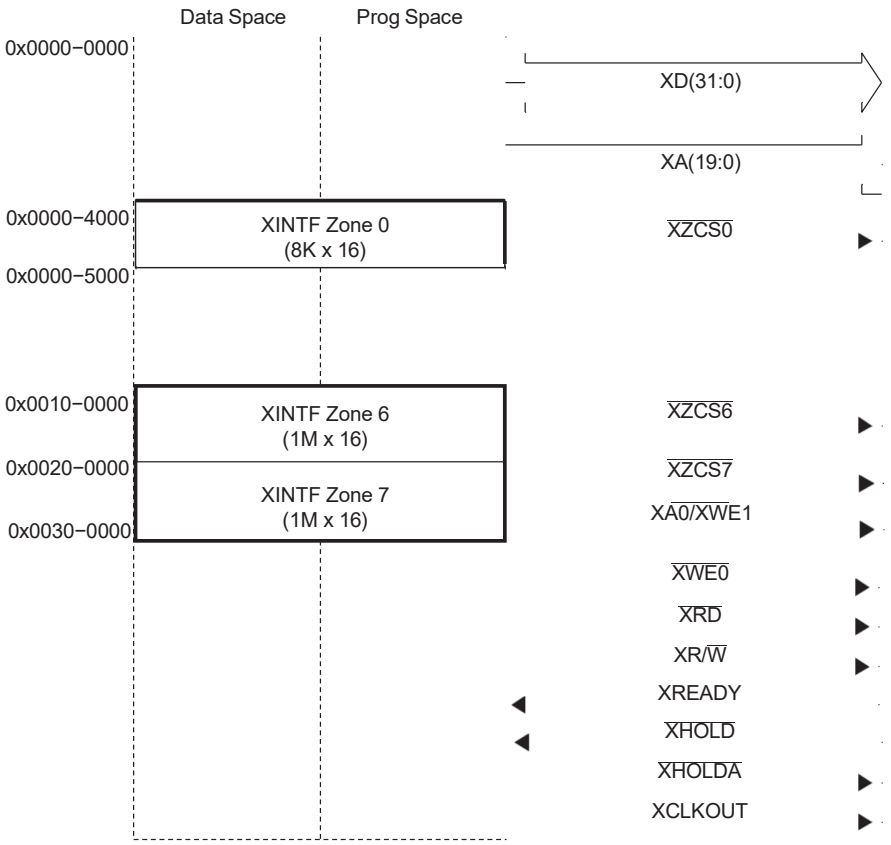
1.1.2 Accessing XINTF Zones

An XINTF zone is a region in the 28x memory map that is directly connected to the external interface. Section 1.1.3 shows zone locations. The memory or peripheral attached to a zone can be accessed directly with the CPU or Code Composer Studio.

Each XINTF zone can be individually configured with unique read and write access timing and each has an associated zone chip-select signal. This chip-select signal is pulled low so that an access to that zone is currently taking place. On 2833x devices, all zone chip select signals are independent.

The external address bus, XA, is 20 bits wide and is shared by all of the zones. What external addresses are generated depends on which zones are being accessed, as follow:

- Zone 0 uses external addresses 0x00000 - 0x00FFF. That is, an access to the first location in Zone 0 will issue external addresses 0x00000 along with chip select 0 (XZCS0). An access to the last location in the zone will issue address 0x00FFF with XZCS0.
- Zone 6 and 7 both use external addresses 0x00000 - 0xFFFFF. Depending on which zone is accessed, the appropriate zone chip select signal (XZCS6 or XZCS7) will also go low.



A Each zone can be programmed with different wait states, setup and hold timings. A dedicated zone chip select ($\overline{\text{XZCS}}$) signal toggles when an access to a particular zone is performed. These features enable glueless connection to many external memories and peripherals.

B Zones 1 – 5 are reserved for future expansion.

C Zones 0, 6, and 7 are always enabled.

1.1.4 Write-Followed-by-Read Pipeline Protection

In the 28x CPU pipeline, the read phase of an operation occurs before the write phase. Due to this ordering, a write followed by a read access can actually occur in the opposite order: read followed by write.

For example, the following lines of code perform a write to one location followed by a read from another. Due to the 28x CPU pipeline, the read operation will be issued before the write as shown:

```
MOV   @REG1,AL
TBIT  @REG2,#BIT_X  ---> Read
                    ---> Write
```

On 28x devices, regions of memory where peripheral registers are common are protected from this order reversal by hardware. These regions of memory are said to be read-followed-by-write pipeline protected. XINTF Zone 0 is by default read-followed-by-write pipeline protected. Write and read accesses to Zone 0 are executed in the same order that they are written. For example, a write followed by a read is executed in the same order it was written as shown below:

```
MOV   @REG1,AL
TBIT  @REG2,#BIT_X  ---> Write
                    ---> Read
```

The 28x CPU automatically protects writes followed by reads to the same memory location. The protection mechanism described above is for cases where the address is not the same, but within a given region of protected memory. In this case, the order of execution is preserved by the CPU automatically inserting enough NOP cycles for the write to complete before the read occurs.

This execution ordering becomes a concern only when peripherals are mapped to the XINTF. A write to one register may update status bits in another register. In this case, the write to the first register must finish before the read to the second register takes place. If the write and read operations are performed in the natural pipeline order, the wrong status may be read since the write would happen after the read. This reversal is not a concern when memory is mapped to the XINTF. Thus, Zone 0 would not typically be used to access memory but instead would be used only to access external peripherals.

If other zones are used to access peripherals that require write-followed-by-read instruction order to be preserved the following solutions can be used:

- Add up to 3 NOP assembly instructions between a write and read instructions. Fewer than three can be used if the code is analyzed and it is found that the pipeline stalls for other reasons.
- Move other instructions before the read to make sure that the write and read are at least three CPU cycles apart.
- Use the -mv compiler option to automatically insert NOP assembly instructions between write and read accesses. This option should be used with caution because this out-of-order execution is a concern only when accessing peripherals mapped to XINTF and not normal memory accesses.

1.2 XINTF Configuration Overview

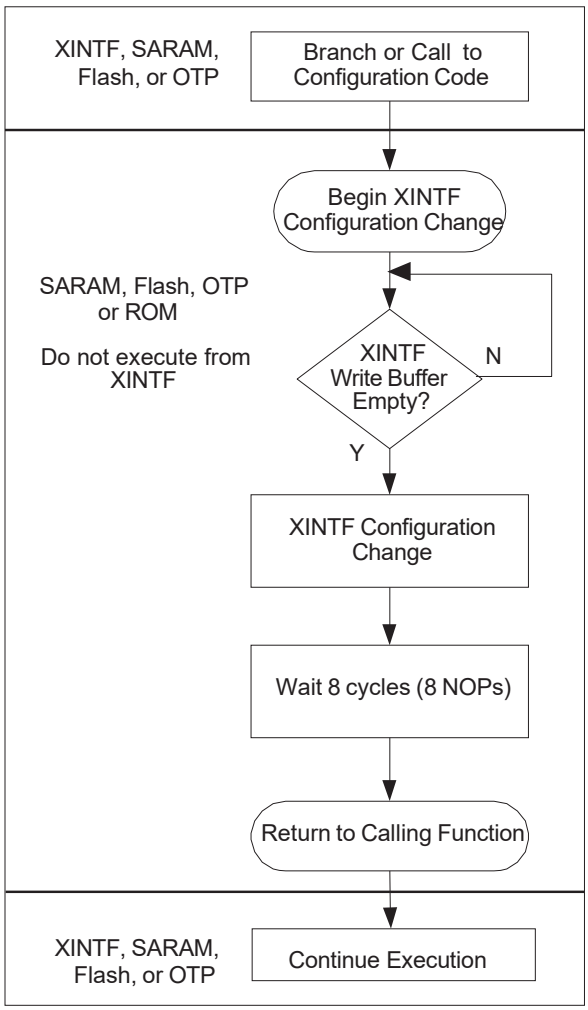
This section is an overview of the XINTF parameters that can be configured to fit particular system requirements. The exact configuration used depends on the operating frequency of the 28x, switching characteristics of the XINTF, and the timing requirements of the external devices. Detailed information on each of these parameters is given in the following sections.

Because a change to the XINTF configuration parameters will cause a change to the access timing, code that configures these parameters should not execute from the XINTF itself.

1.2.1 Procedure to Change the XINTF Configuration and Timing Registers

During an XINTF configuration or timing change no accesses to the XINTF can be in progress. This includes instructions still in the CPU pipeline, write accesses in the XINTF write buffer, data reads or writes, instruction pre-fetch operations and DMA accesses. To be sure that no access takes place during the configuration follow these steps:

1. Make sure that the DMA is not accessing the XINTF.
2. Follow the procedure shown in Section 1.2.2 to safely modify the XTIMING0/6/7, XBANK, or F2 registers.



Branch or call is required to properly flush the CPU pipeline before the configuration change.

The function that changes the configuration cannot execute from the XINTF.

The XINTF write buffer must be empty before the configuration change.

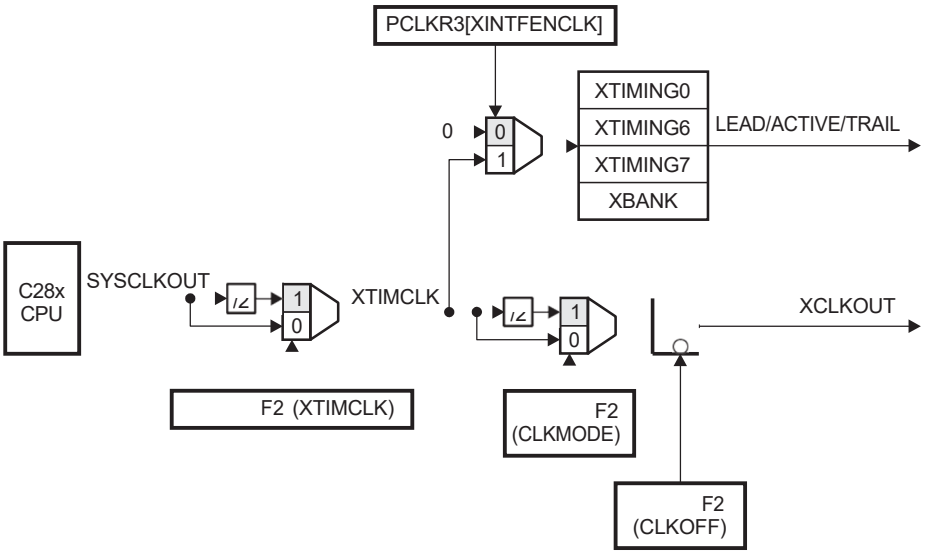
The stack must not be in external memory.

Write instructions to XTIMING0/6/7, XBANK, or F2

Wait eight cycles to let the write instructions propogate through the CPU pipeline. This must be done before the return-from-function call is made.

1.2.3 XINTF Clocking

There are two clocks used by the XINTF module: XTIMCLK and XCLKOUT. Section 1.2.4 shows the relationship between these two clocks and the CPU clock, SYSCLKOUT.



All accesses to all of the XINTF zones are based on the frequency of the internal XINTF clock, XTIMCLK. When configuring the XINTF, you must choose the ratio for the internal XINTF clock, XTIMCLK, with respect to SYSCLKOUT. XTIMCLK can be configured to be either equal or one half of SYSCLKOUT by writing to the XTIMCLK bit in the F2 register. By default XTIMCLK is one-half of SYSCLKOUT.

All XINTF accesses begin on the rising edge of the external clock out, XCLKOUT. In addition, external logic may be clocked off of XCLKOUT. The frequency of XCLKOUT can be configured as a ratio of the internal XINTF clock, XTIMCLK. XCLKOUT can be configured to be either equal or one-half of XTIMCLK by writing to the CLKMODE bit in the F2 register. By default, XCLKOUT is one-half of XTIMCLK, or one-fourth of the CPU clock, SYSCLKOUT.

To reduce system noise, you may choose to not output XCLKOUT on a pin. This is done by writing a 1 to the F2[CLKOFF] bit.

1.2.5 Write Buffer

By default, write access buffering is disabled. In most cases, to improve performance of the XINTF, you should enable write buffering. Up to three writes to the XINTF can be buffered without stalling the CPU. The write buffer depth is configured in the F2 register.

1.2.6 XINTF Access Lead/Active/Trail Wait-State Timing Per Zone

An XINTF zone is a region of memory-mapped addresses that directly access the external interface. The timing of any read or write access to an XINTF zone can be divided into the following three portions: Lead, Active, and Trail. The number of XTIMCLK cycle wait states for each portion of an access can be configured for each XINTF zone in the corresponding zone XTIMING register. Timing for read accesses can be configured separately from timing for write accesses. In addition, to facilitate connections to slow external devices the X2TIMING bit can be used to double the specified lead/active and trail wait states for a particular zone.

During the lead portion, the chip-select signal for the zone being accessed is taken low and the address is placed on the address bus (XA). The total lead period, in XTIMCLK cycles can be configured in the zone's XTIMING register. By default, the lead period is set to the maximum six XTIMCLK cycles for both read and write accesses.