AK8963

3-axis Electronic Compass

1. Features

A 3-axis electronic compass IC with high sensitive Hall sensor technology.
Best adapted to pedestrian city navigation use for cell phone and other portable appliance.

Functions:

- 3-axis magnetometer device suitable for compass application
- Built-in A to D Converter for magnetometer data out
- 14-/16-bit selectable data out for each 3 axis magnetic components
  - Sensitivity: 0.6 µT/LSB typ. (14-bit)
    0.15µT/LSB typ. (16-bit)
- Serial interface
  - I^2C bus interface.
    Standard mode and Fast mode compliant with Philips I^2C specification Ver.2.1
  - 4-wire SPI
- Operation modes:
  Power-down, Single measurement, Continuous measurement, External trigger measurement, Self test and Fuse ROM access.
- DRDY function for measurement data ready
- Magnetic sensor overflow monitor function
- Built-in oscillator for internal clock source
- Power on Reset circuit
- Self test function with built-in internal magnetic source

Operating temperatures:

- -30°C to +85°C

Operating supply voltage:

- Analog power supply +2.4V to +3.6V
- Digital Interface supply +1.65V to analog power supply voltage.

Current consumption:

- Power-down: 3 µA typ.
- Measurement:
  - Average power consumption at 8 Hz repetition rate: 280µA typ.

Package:

AK8963C 14-pin WL-CSP (BGA): 1.6 mm × 1.6 mm × 0.5 mm (typ.)
AK8963N 16-pin QFN package: 3.0 mm × 3.0 mm × 0.75 mm (typ.)

2. Overview

AK8963 is 3-axis electronic compass IC with high sensitive Hall sensor technology.
Small package of AK8963 incorporates magnetic sensors for detecting terrestrial magnetism in the X-axis, Y-axis, and Z-axis, a sensor driving circuit, signal amplifier chain, and an arithmetic circuit for processing the signal from each sensor. Self test function is also incorporated. From its compact foot print and thin package feature, it is suitable for map heading up purpose in GPS-equipped cell phone to realize pedestrian navigation function.

AK8963 has the following features:

(1) Silicon monolithic Hall-effect magnetic sensor with magnetic concentrator realizes 3-axis magnetometer on a silicon chip. Analog circuit, digital logic, power block and interface block are also integrated on a chip.

(2) Wide dynamic measurement range and high resolution with lower current consumption.

Output data resolution:	14-bit (0.6 μT/LSB)
	16-bit (0.15 μT/LSB)
Measurement range:	± 4900 μT
Average current at 8Hz repetition rate:	280μA typ.

(3) Digital serial interface
- I^2C bus interface to control AK8963 functions and to read out the measured data by external CPU. A dedicated power supply for I^2C bus interface can work in low-voltage apply as low as 1.65V.
- 4-wire SPI is also supported. A dedicated power supply for SPI can work in low-voltage apply as low as 1.65V.

(4) DRDY pin and register inform to system that measurement is end and set of data in registers are ready to be read.

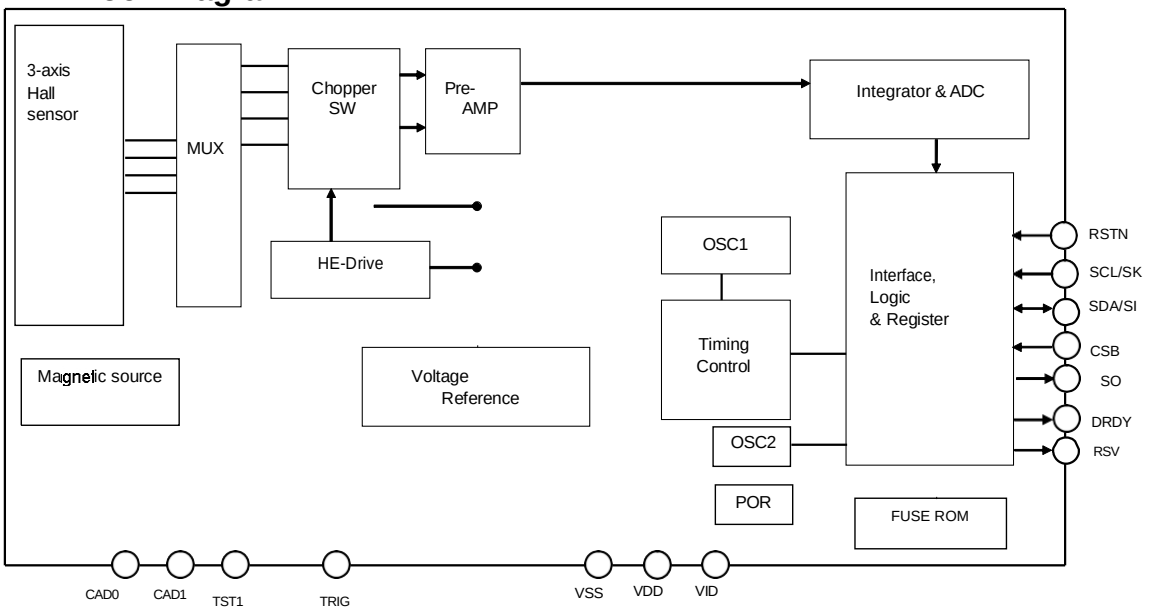
(5) Device is worked by on-chip oscillator so no external clock source is necessary.

(6) Self test function with internal magnetic source to confirm magnetic sensor operation on end products.

3. Table of Contents

4. Circuit Configuration

4.1. Block Diagram



4.2. Block Function

Block	Function
3-axis Hall sensor	Monolithic Hall elements.
MUX	Multiplexer for selecting Hall elements.
Chopper SW	Performs chopping.
HE-Drive	Magnetic sensor drive circuit for constant-current driving of sensor
Pre-AMP	Fixed-gain differential amplifier used to amplify the magnetic sensor signal.
Integrator & ADC	Integrates and amplifies pre-AMP output and performs analog-to-digital conversion.
OSC1	Generates an operating clock for sensor measurement. 12MHz(typ.)
OSC2	Generates an operating clock for sequencer. 128kHz(typ.)
POR	Power On Reset circuit. Generates reset signal on rising edge of VDD.
Interface Logic & Register	Exchanges data with an external CPU. DRDY pin indicates sensor measurement end and data is ready to be read. I^2C bus interface using two pins, namely, SCL and SDA. Standard mode and Fast mode are supported. The low-voltage specification can be supported by applying 1.65V to the VID pin. 4-wire SPI is also supported by SK, SI, SO and CSB pins. 4-wire SPI works in VID pin voltage down to 1.65V, too.
Timing Control	Generates a timing signal required for internal operation from a clock generated by the OSC1.
Magnetic Source	Generates magnetic field for self test of magnetic sensor.
FUSE ROM	Fuse for adjustment

4.3. Pin Function

QFN Pin No.	WLCSP Pin No.	Pin name	I/O	Power supply system	Type	Function
1	A1	DRDY	O	VID	CMOS	Data Ready output pin. "H" active. Informs measurement ended and data is ready to be read.
2	A2	CSB	I	VID	CMOS	Chip select pin for 4-wire SPI. "L" active. Connect to VID when selecting I^2C bus interface.
3	A3	SCL	I	VID	CMOS	When the I^2C bus interface is selected (CSB pin is connected to VID) SCL: Control data clock input pin Input: Schmidt trigger
		SK				When the 4-wire SPI is selected SK: Serial clock input pin
5	A4	SDA	I/O	VID	CMOS	When the I^2C bus interface is selected (CSB pin is connected to VID) SDA: Control data input/output pin Input: Schmidt trigger, Output: Open drain
		SI	I			When the 4-wire SPI is selected SI: Serial data input pin
15	B1	VDD	-	-	Power	Analog Power supply pin.
4	B3	RSV	O	VID	CMOS	Reserved. Keep this pin electrically non-connected.
6	B4	SO	O	VID	CMOS	When the I^2C bus interface is selected (CSB pin is connected to VID) Hi-Z output. Keep this pin electrically non-connected.
						When the 4-wire SPI is selected Serial data output pin
13	C1	VSS	-	-	Power	Ground pin.
14	C2	TST1	I	VDD	CMOS	Test pin. Pulled down by 100kΩ internal resister. Keep this pin electrically non-connected or connect to VSS.
7	C3	TRG	I	VID	CMOS	External trigger pulse input pin. Enabled only in External trigger mode. Pulled down by 100kΩ internal resister. When External trigger mode is not in use, keep this pin electrically non-connected or connect to VSS.
8	C4	VID	-	-	Power	Digital interface positive power supply pin.
12	D1	CAD0	I	VDD	CMOS	When the I^2C bus interface is selected (CSB pin is connected to VID) CAD0: Slave address 0 input pin Connect to VSS or VDD.
						When the 4-wire serial interface is selected Connect to VSS.
11	D2	CAD1	I	VDD	CMOS	When the I^2C bus interface is selected (CSB pin is connected to VID) CAD1: Slave address 1 input pin Connect to VSS or VDD.
						When the 4-wire serial interface is selected Connect to VSS.
10	D4	RSTN	I	VID	CMOS	Reset pin. Resets registers by setting to "L". Connect to VID when not in use.

5. Overall Characteristics

5.1. Absolute Maximum Ratings

Vss=0V

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage (Vdd, Vid)	V+	-0.3	+4.3	V
Input voltage	VIN	-0.3	(V+)+0.3	V
Input current	IIN	-	±10	mA
Storage temperature	TST	-40	+125	°C

(Note 1) If the device is used in conditions exceeding these values, the device may be destroyed. Normal operations are not guaranteed in such exceeding conditions.

5.2. Recommended Operating Conditions

Vss=0V

Parameter	Remark	Symbol	Min.	Typ.	Max.	Unit
Operating temperature		Ta	-30		+85	°C
Power supply voltage	VDD pin voltage	Vdd	2.4	3.0	3.6	V
	VID pin voltage	Vid	1.65		Vdd	V

5.3. Electrical Characteristics

The following conditions apply unless otherwise noted:
Vdd=2.4V to 3.6V, Vid=1.65V to Vdd, Temperature range=-30°C to 85°C

5.3.1. DC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level input voltage 1	VIH1	CSB RSTN TRG		70%Vid			V
Low level input voltage 1	VIL1					30%Vid	V
High level input voltage 2	VIH2	SK/SCL SI/SDA		70%Vid		Vid+0.5	V
Low level input voltage 2	VIL2			-0.5		30%Vid	V
High level input voltage 3	VIH3	CAD0 CAD1		70%Vdd			V
Low level input voltage 3	VIL3					30%Vdd	V
Input current 1	IIN1	SK/SCL SI/SDA CSB RSTN	Vin=Vss or Vid	-10		+10	μA
Input current 2	IIN2	CAD0 CAD1	Vin=Vss or Vdd	-10		+10	μA
Input current 3	IIN3	TRG	Vin=Vid			100	μA
Input current 4	IIN4	TST1	Vin=Vdd			100	μA
Hysteresis input voltage (Note 2)	VHS	SCL SDA	Vid≥2V	5%Vid			V
			Vid<2V	10%Vid			V
High level output voltage 1	VOH1	SO DRDY	IOH≥-100μA	80%Vid			V
Low level output voltage 1	VOL1		IOL≤+100μA			20%Vid	V
Low level output voltage 2 (Note 3)(Note 4)	VOL2	SDA	IOL≤3mA Vid≥2V			0.4	V
			IOL≤3mA Vid<2V			20%Vid	V
Current consumption (Note 5)	IDD1	VDD VID	Power-down mode Vdd=Vid=3.0V		3	10	μA
	IDD2		When magnetic sensor is driven		5	10	mA
	IDD3		Self-test mode		9	15	mA
	IDD4		(Note 6)		0.1	5	μA

(Note 2) Schmitt trigger input (reference value for design)
(Note 3) Maximum load capacitance: 400pF (capacitive load of each bus line applied to the I^2C bus interface)
(Note 4) Output is open-drain. Connect a pull-up resistor externally.
(Note 5) Without any resistance load
(Note 6) (case1)Vdd=ON, Vid=ON, RSTN pin = "L". (case2)Vdd=ON, Vid=OFF(0V),RSTN pin = "L".

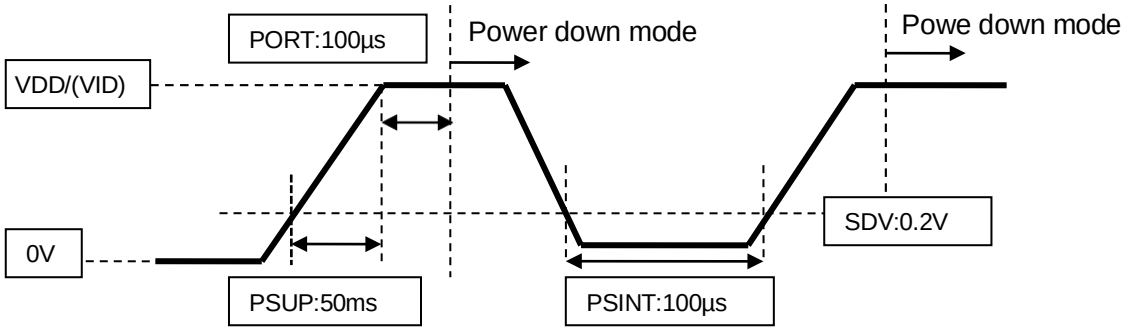
(case3)Vdd=Off(0V), Vid=On.

5.3.2. AC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply rise time (Note 7)	PSUP	VDD VID	Period of time that VDD (VID) changes from 0.2V to Vdd (Vid). (Note 8)			50	ms
POR completion time (Note 7)	PORT		Period of time after PSUP to Power-down mode (Note 8)			100	µs
Power supply turn off voltage	SDV	VDD VID	Turn off voltage to enable POR to restart (Note 8)			0.2	V
Power supply turn on interval (Note 7)	PSINT	VDD VID	Period of time that voltage lower than SDV needed to be kept to enable POR to restart (Note 8)	100			µs
Wait time before mode setting	Twat			100			µs

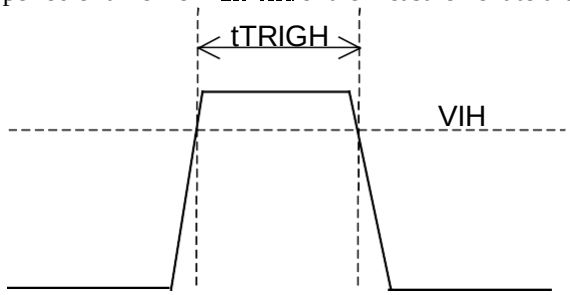
(Note 7) Reference value for design

(Note 8) When POR circuit detects the rise of VDD/VID voltage, it resets internal circuits and initializes the registers. After reset, AK8963 transits to Power-down mode.

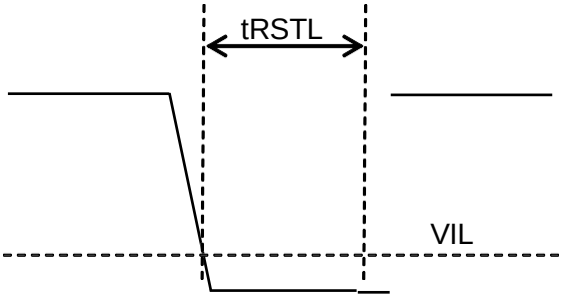


Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Trigger input effective pulse width	tTRIGH	TRG		200			ns
Trigger input effective frequency (Note 9)	tTRIGf	TRG				100	Hz

(Note 9) The value when the period of time from the end of the measurement to the next trigger input is 1.3ms.



Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Reset input effective pulse width (“L”)	tRSTL	RSTN		5			μs



5.3.3. Analog Circuit Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Measurement data output bit	DBIT	BIT = “0”		14		bit
		BIT = “1”		16		
Time for measurement	TSM	Single measurement mode		7.2	9	ms
Magnetic sensor sensitivity	BSE	Tc=25°C (Note 10)				
		BIT = “0”	0.57	0.6	0.63	μT/LSB
		BIT = “1”	0.1425	0.15	0.1575	
Magnetic sensor measurement range (Note 11)	BRG	Tc=25°C (Note 10)	±4912			μT
Magnetic sensor initial offset (Note 12)		Tc=25°C BIT = “0”	-500		500	LSB

(Note 10) Value after sensitivity is adjusted using sensitivity fine adjustment data stored in Fuse ROM. (Refer to 8.3.11 for how to adjust.)
(Note 11) Reference value for design
(Note 12) Value of measurement data register on shipment without applying magnetic field on purpose.

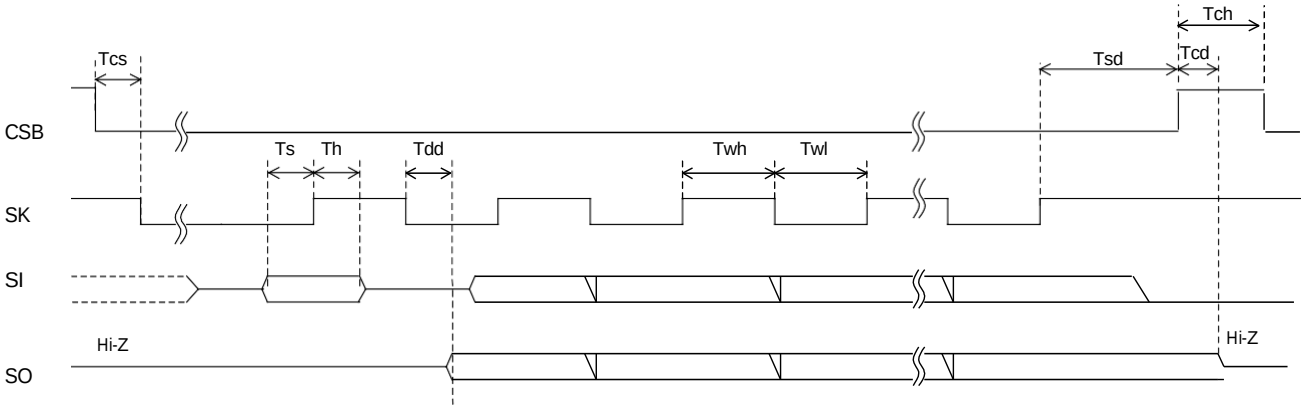
5.3.4. 4-wire SPI

4-wire SPI is compliant with mode 3

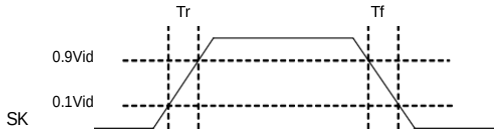
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CSB setup time	Tcs		50			ns
Data setup time	Ts		50			ns
Data hold time	Th		50			ns
SK high time	Twh	Vid≥2.5V	100			ns
		2.5V>Vid≥1.65V	150			ns
SK low time	Twl	Vid≥2.5V	100			ns
		2.5V>Vid≥1.65V	150			ns
SK setup time	Tsd		50			ns
SK to SO delay time (Note 13)	Tdd				50	ns
CSB to SO delay time (Note 13)	Tcd				50	ns
SK rise time (Note 14)	Tr				100	ns
SK fall time (Note 14)	Tf				100	ns
CSB high time	Tch		150			ns

(Note 13) SO load capacitance: 20pF
(Note 14) Reference value for design.

[4-wire SPI]



[Rise time and fall time]



5.3.5. I²C Bus Interface

CSB pin = "H"

I²C bus interface is compliant with Standard mode and Fast mode. Standard/Fast mode is selected automatically by fSCL.

(1) Standard mode

fSCL≤100kHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			100	kHz
tHIGH	SCL clock "High" time	4.0			µs
tLOW	SCL clock "Low" time	4.7			µs
tR	SDA and SCL rise time			1.0	µs
tF	SDA and SCL fall time			0.3	µs
tHD:STA	Start Condition hold time	4.0			µs
tSU:STA	Start Condition setup time	4.7			µs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0			µs
tSU:DAT	SDA setup time (vs. SCL rising edge)	250			ns
tSU:STO	Stop Condition setup time	4.0			µs
tBUF	Bus free time	4.7			µs

(2) Fast mode

100kHz<fSCL≤400kHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			400	kHz
tHIGH	SCL clock "High" time	0.6			µs
tLOW	SCL clock "Low" time	1.3			µs
tR	SDA and SCL rise time			0.3	µs
tF	SDA and SCL fall time			0.3	µs
tHD:STA	Start Condition hold time	0.6			µs
tSU:STA	Start Condition setup time	0.6			µs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0			µs
tSU:DAT	SDA setup time (vs. SCL rising edge)	100			ns
tSU:STO	Stop Condition setup time	0.6			µs
tBUF	Bus free time	1.3			µs
tSP	Noise suppression pulse width			50	ns

[I²C bus interface timing]