Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Spring 2007

Lab 2: MOSFET Inverting Amplifiers & First-Order Circuits
Handout S07-034

Introduction

This lab examines the behavior of an inverting MOSFET amplifier. It begins by examining the static input-output relation of the amplifier, and concludes by examining the dynamic behavior of the same amplifier when used as a digital logic inverter. You should complete the pre-lab exercises in your lab notebook before coming to lab. Then, carry out the in-lab exercises between April 2 and April 6. After completing the in-lab exercises, have a TA or LA check your work and sign your lab notebook. Before asking to get checked off, make sure you meet all the requirements in the checkoff list at the end of the In-Lab Exercises. Finally, complete the post-lab exercises in your lab notebook, and turn in your lab notebook on or before Wednesday, April 11.

Bring in your favorite CD for In-Lab Exercise 2-3; it is meant to be a fun experiment and its results will not be needed for the post lab exercises. If you have a portable CD player or laptop, please bring that for use in In-Lab Exercise 2-3, as the stockroom has only a limited number of CD players and speakers available.

Pre-Lab Exercises

(2-1) Consider the inverting MOSFET amplifier shown in Figure 1. Using the SCS MOSFET model, write an expression for v_{OUT} as a function of v_{IN} for $0 \le v_{IN} \le v_{OUT} + V_{TM}$. Note that V_{TM} is the threshold voltage of the MOSFET. Also, sketch and clearly label the form of v_{OUT} as a function of v_{IN} over the same range.

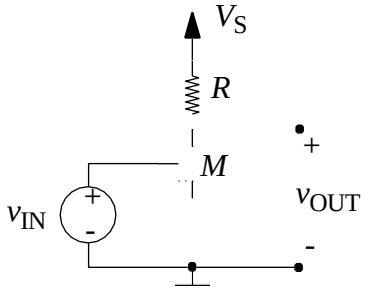

Figure 1: Inverting MOSFET amplifier for Pre-Lab Exercises 2-1 and 2-2.

(2-2) Write an expression for the small-signal gain of the MOSFET amplifier shown in Figure 1 assuming that the MOSFET is biased into saturated operation.

(2-3) Consider the network shown in Figure 2. First, assume that $v_{OUT} = 0$ at time $t = 0$. Then, write an expression for $v_{OUT}(t)$ for $t \ge 0$ given that v_{IN} steps from 0 V to V_I at $t = 0$.

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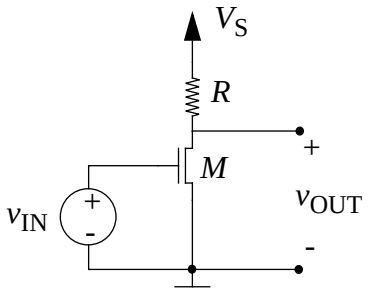

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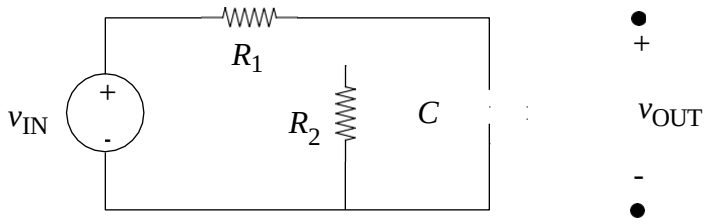


Figure 2: Network for Pre-Lab Exercises 2-3 and 2-4.

(2-4) For the transient determined in Pre-Lab Exercise 2-3, determine the time at which v_{OUT} reaches a given V_T where $0 < V_T < \frac{R_2}{R_1+R_2} V_I$.

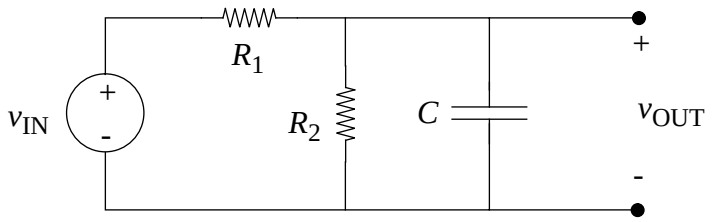
(2-5) (OPTIONAL) Design Competition: Design an inverter with the minimum power-delay product that meets the following static discipline: $V_{OH} = 4.8V$, $V_{OL} = 0.1V$, $V_{IH} = 2.5V$, $V_{IL} = 0.3V$. Power-delay product is the product of the static power dissipated when the MOSFET is on, and the time the output voltage takes to rise from your inverter's low output to V_{OH}. Also, assume that your inverter is driving a load capacitance of $C_L = 97pF$, that $V_T = 1.8V$, and $R_{DS-ON} = 2\Omega$.

In order to be considered for the competition, you must turn in the following with your post-lab:

1. A circuit diagram of your inverter, with values for R_L and V_S clearly specified.
2. A description (accompanied by the appropriate equations) showing how your values minimize the power-delay product, and how you reached those values.
3. Predicted values for the power-delay product using your values for V_S and R_L, and using $V_S = 5V$ and your value of R_L.
4. A comparison between your predicted value from 3 and your measured value from In-Lab Exercise 2-4. If there are large discrepancies, try recalculating your power-delay product based on the value for C_L you calculated in Post-Lab Exercise 3.

Make sure to read the description for In-Lab Exercise 2-4. Those doing the competition will need to do this exercise slightly differently.

Finally, make sure to keep your design competition write-up separate from your post-lab (i.e. the write-up should not be written in your lab notebook). Hand in your competition write-up to your recitation TA on or before Wednesday, April 11. First prize is dinner in a fancy restaurant with the 6.002 staff.



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In-Lab Exercises

As part of the in-lab exercises, you will measure the threshold voltage and gate-to-source capacitance of a MOSFET. Because these parameters will not be identical for different 2N7000 MOSFETs, try to use the same MOSFET for the MOSFET labeled as *M* in every in-lab exercise described below. Remember that the MOSFET should say 2N7000 on it.

(2-1)

(a) This exercise measures the static input-output relation of the MOSFET amplifier shown in Figure 1. To begin, construct the amplifier as shown in Figure 3, and connect the signal generator and oscilloscope as shown. Next, set the signal generator to produce a 1-kHz sine wave with a peak-to-peak amplitude of 3 V and an offset of 1.5 V. Thus, the signal generator will produce a biased sine wave between 0 V and 3 V. Set the oscilloscope to operate in its X-Y mode with an X-axis (Channel #1) sensitivity of 500 mV per division and a Y-axis (Channel #2) sensitivity of 1 V per division. To set the oscilloscope in X-Y mode, turn the *SEC/DIV* knob all the way to the left. You should now see the input-output relation and on the oscilloscope. Make a sketch in your notebook of this input-output relation and note any difference between this relation and the input-output relation you calculated for Pre-Lab Exercise 2-1.

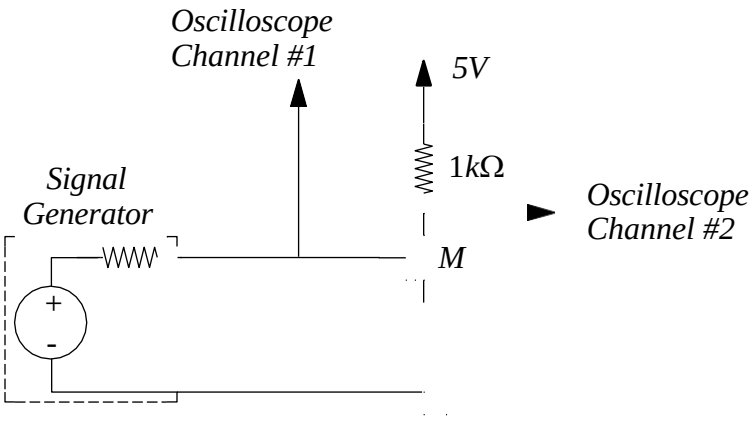

Figure 3: Measuring the static input-output relation of the MOSFET amplifier shown in Figure 1.

You may find it easier and much more accurate to use the signal generator as a programmable v_{IN} source and measure v_{OUT} with a multimeter for parts (b) and (c).

(b) Record the value of v_{IN} above which v_{OUT} just begins to fall. This is the threshold voltage V_{TM} of the MOSFET (see the sketch from Pre-Lab Exercise 2-1).

(c) Record the values of v_{IN} which correspond to v_{OUT} values of 5 V, 4 V, 3 V, 2 V and 1 V.

(2-2) This exercise measures the small-signal gain of the amplifier shown in Figure 1 when its output operating-point voltage is 2 V. Construct Circuit #1 shown in Figure 4. Adjust the potentiometer until v_{OUT} = 2 V as measured by the multimeter. Connect the signal generator and the oscilloscope as shown in Circuit #2. Set the signal generator to zero and re-adjust the potentiometer so that v_{OUT} = 2 V. Then, set the signal generator to produce an unbiased 1-kHz sine wave with a peak-to-peak amplitude of 100 mV. Measure

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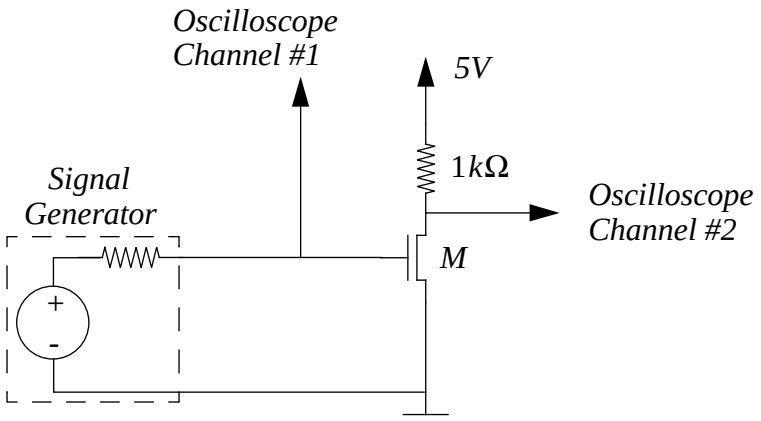

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the amplitude of both v_{in} and v_{out}, which are the sinusoidal components of v_{IN} and v_{OUT}, respectively (use AC coupling in Channel #1 of the oscilloscope to accurately measure v_{in}). The ratio of the amplitudes is the small-signal gain. Retain this circuit for the next exercise.

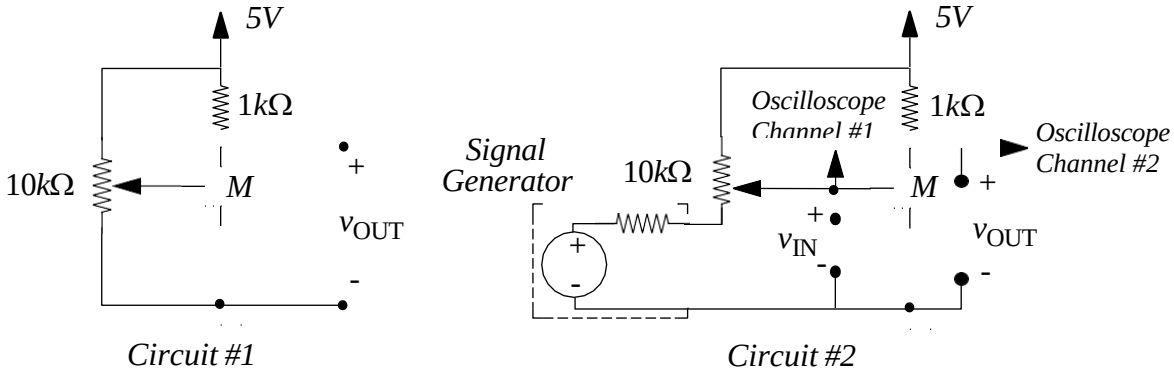


Figure 4: Measuring the small-signal gain of the MOSFET amplifier.

(2-3) The experiments in this exercise will use Circuit #2 constructed in In-Lab Exercise 2-2 to explore the limits of saturation operation of the amplifier by observing clipping of an output waveform and by listening to distortion in music output.

(a) Start by adjusting the input bias with the potentiometer, and observing the variation in v_{OUT}. Now, increase the peak-to-peak amplitude of the sine wave input from the signal generator to 300 mV. Observing the output on Channel #2 of the oscilloscope, increase the input bias voltage until you see clipping on the bottom part of the output. Use DC coupling in Channel #1 of the oscilloscope and make a note of the upper excursion limit of the voltage v_{IN} (the maximum input voltage before clipping occurs). Similarly, decrease the input bias voltage until you see clipping on the top part of the output, and make a note of the lower excursion limit of the voltage v_{IN}. These upper and lower limits of v_{IN} approximate the input operating limits of the amplifier for linear operation.

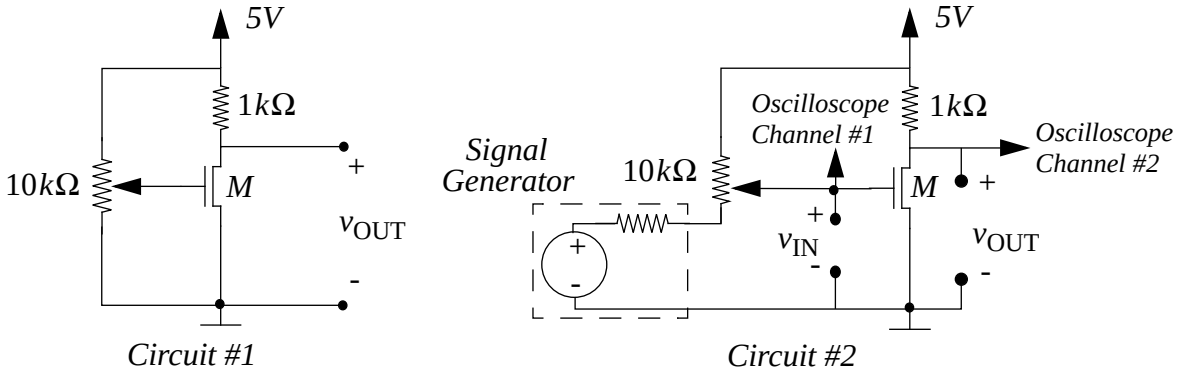
(b) Replace the signal generator with the CD player (use the headphones output). Set the CD player volume such that the peak-to-peak amplitude of the music signal, v_{in}, is approximately 300mV, when viewed on Channel#1. Connect the v_{OUT} signal to an amplifying speaker (leave the oscilloscope connection in place) and adjust the speaker volume to listen to the music. Vary the input bias voltage with the potentiometer and listen to the change in volume. Observing v_{IN} on Channel #1 of the oscilloscope (using DC coupling), increase the input bias voltage until you begin to hear distortion. Is the upper excursion limit of the voltage v_{IN} at the onset of distortion approximately the same as that measured with the sine wave input?

(c) Now, decrease the input bias voltage till you begin to hear distortion. Is the lower excursion limit of the voltage v_{IN} at the onset of distortion approximately the same as that measured with the sine wave input?

(2-4) The next two exercises will analyze the delay of the MOSFET amplifier when it is used as a digital logic inverter. Specifically, we will measure the delay of an inverter that is driving another inverter as illustrated in Figure 6.

Since the delay of an inverter is related to the capacitance of the node that is driven by

the amplitude of both v_{in} and v_{out}, which are the sinusoidal components of v_{IN} and v_{OUT}, respectively (use AC coupling in Channel #1 of the oscilloscope to accurately measure v_{in}). The ratio of the amplitudes is the small-signal gain. Retain this circuit for the next exercise.



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Since the delay of an inverter is related to the capacitance of the node that is driven by

its output, this exercise measures the capacitance seen by the output of an inverter that is driving the gate of a MOSFET.

Construct the circuit shown in Figure 5. You will measure the capacitance C_P seen at node P in the circuit. C_P is the capacitance at node P, and includes C_{GS}, the gate capacitance of MOSFET M, in parallel with the oscilloscope input capacitance and a parasitic wiring capacitance. Set the signal generator to produce a 8-kHz square wave with an amplitude of 5 V peak-to-peak and an offset of 2.5 V. Channel #2 of the oscilloscope should display both a first-order rising step response and a first-order falling step response. Measure the time constant of the rising step response. Since the on resistance of the MOSFET is very small, the falling response has a very small time constant that is difficult to measure. Therefore, we will focus on the rising step response. To measure the time constant of the rising step response, note that the initial slope of the response is as follows:

$$\text{Initial slope of response} = (\text{Final voltage on capacitor} - \text{Initial voltage on capacitor})/\tau \approx \frac{5}{\tau}$$

From your oscilloscope screen, make an estimate of the initial slope, and use that to calculate the τ of the circuit.

For those doing the optional design competition from Pre-Lab Excercise 2-5, instead of using $R_L = 100k\Omega$, use the value of R_L you designed. Also, measure the voltage across R_L when $V_{IN} = 5VDC$ to allow you to calculate the static power dissipated. Please note in your lab notebook if you are taking part in the competition.

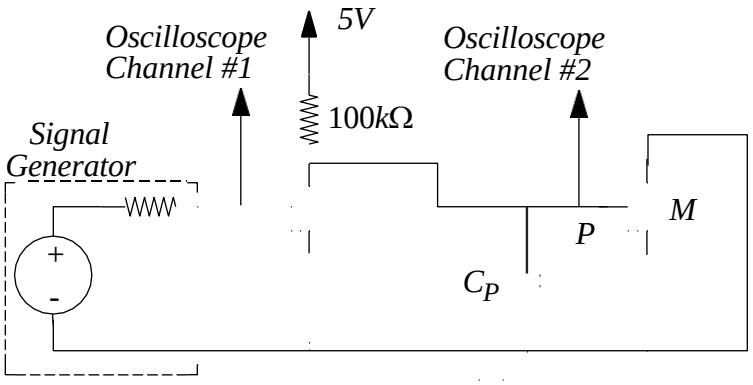

Figure 5: Measuring the gate-to-source capacitance of the MOSFET amplifier.

(2-5) This exercise measures the delay of the MOSFET amplifier when it is used as a digital logic inverter. Construct the circuit shown in Figure 6; As in the previous exercise, set the signal generator to produce a 8-kHz square wave with an amplitude of 5 V peak-to-peak and a DC offset of 2.5 V. Use the oscilloscope to measure the delay from the time at which the signal generator switches low (Channel #1) to the time at which the inverter pair output (Channel #2) begins to switch low. (Note that a high to low transition at the signal generator input corresponds to a low to high transition at node P).

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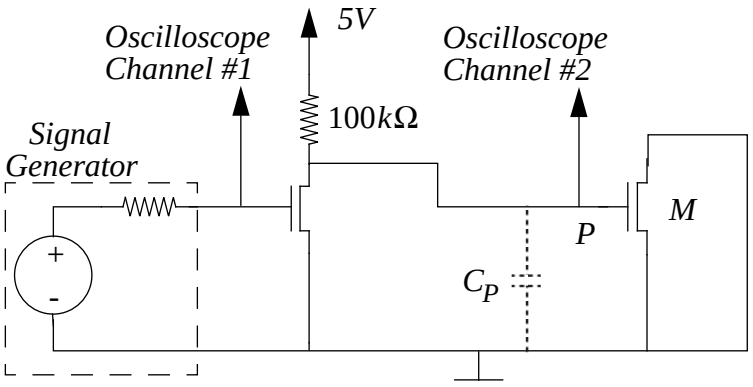

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