PCI-EXPRESS EDGE CONNECTOR

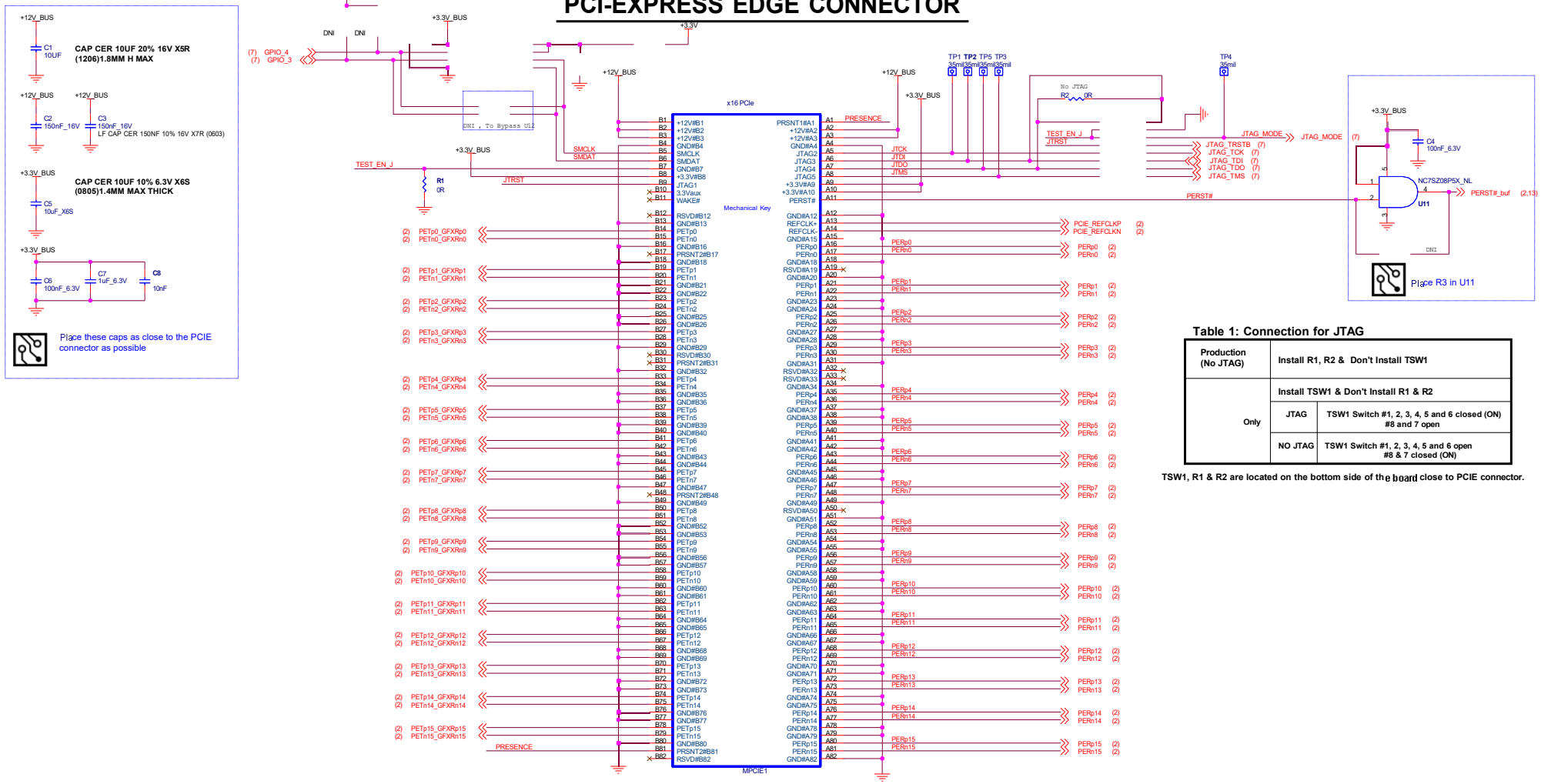

Table 1: Connection for JTAG

Production (No JTAG)	Install R1, R2 & Don't Install TSW1	
Only	Install TSW1 & Don't Install R1 & R2	
	JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open
	NO JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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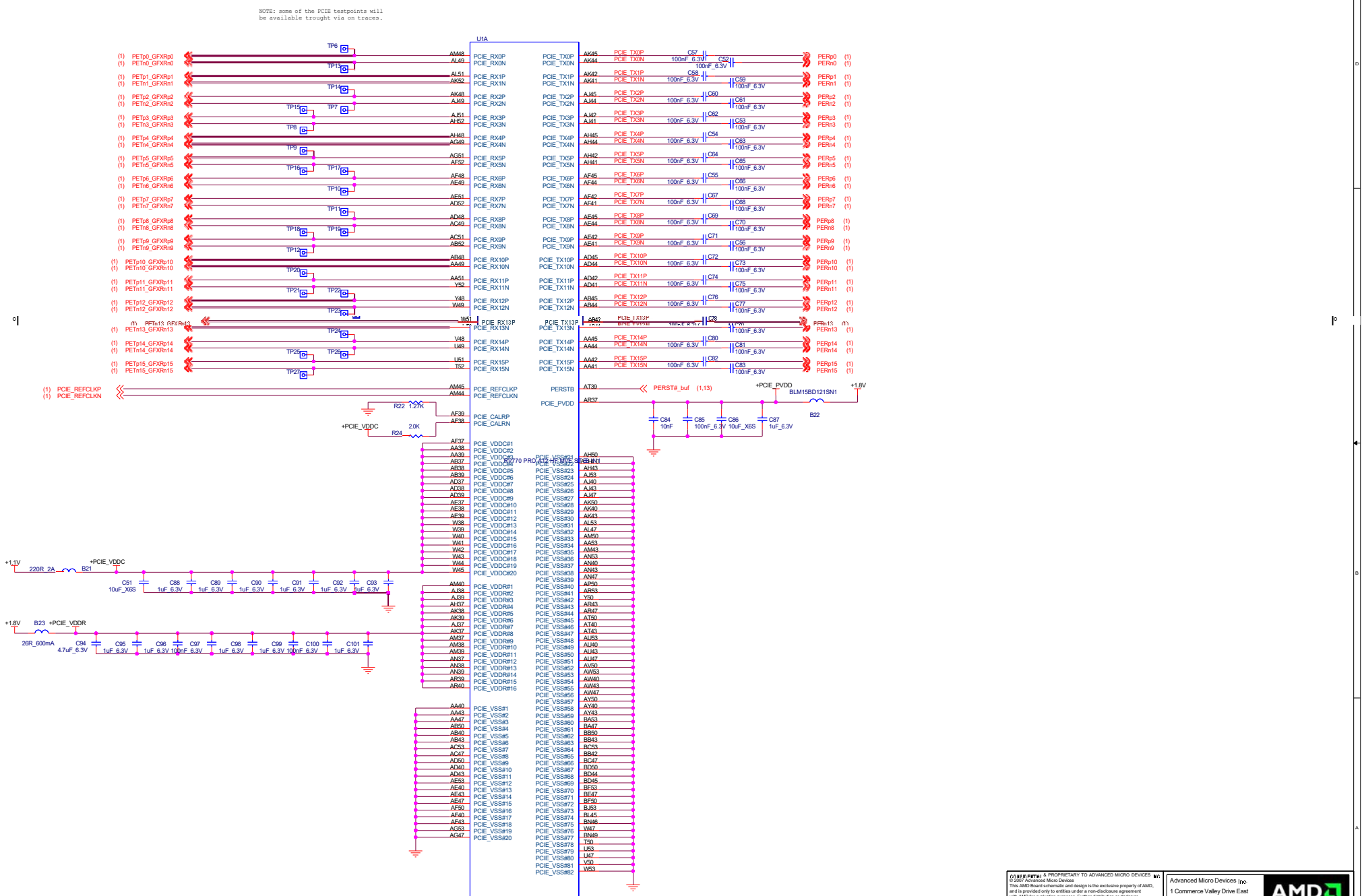
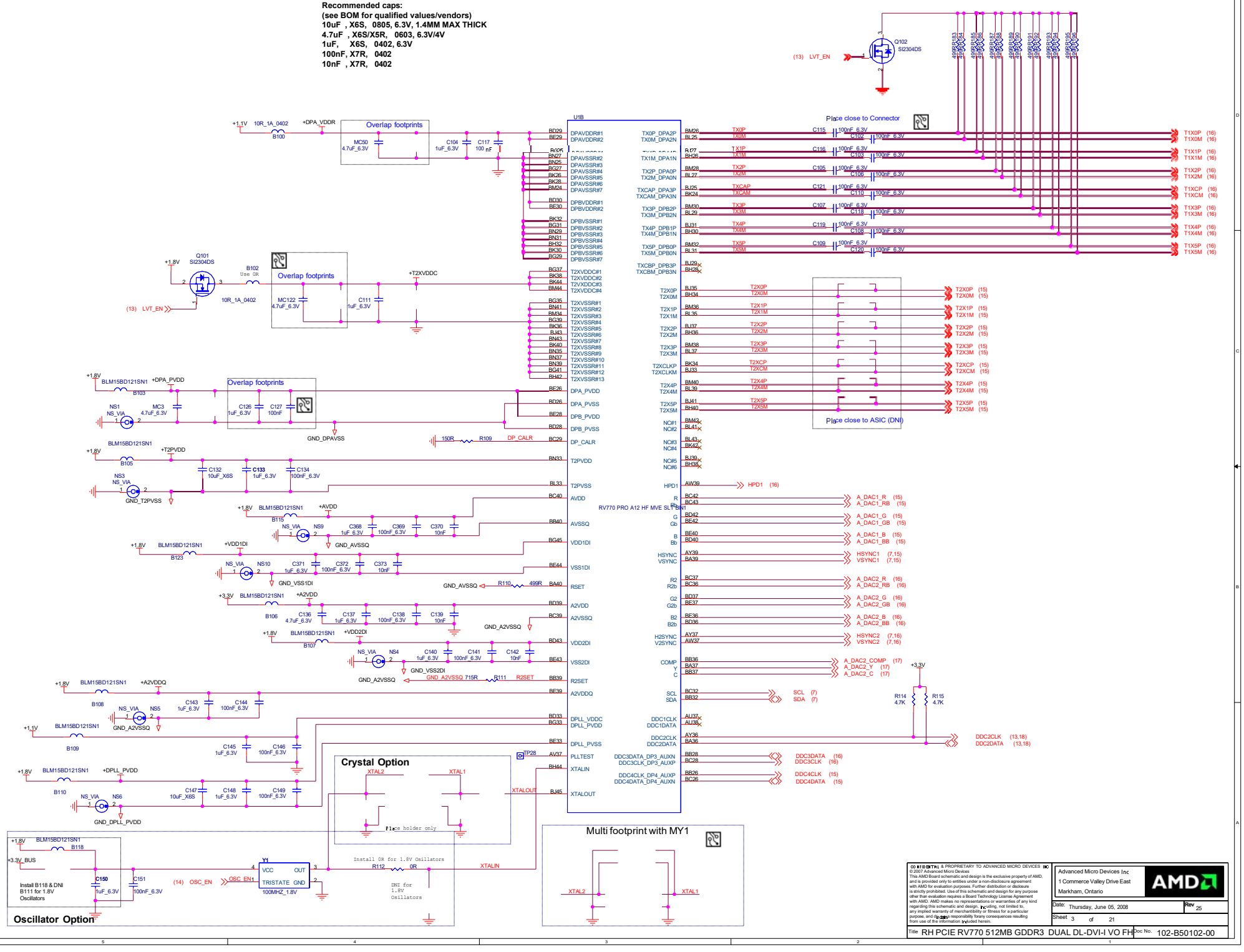


Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
4.7uF , X6S/X5R, 0603, 6.3V/4V
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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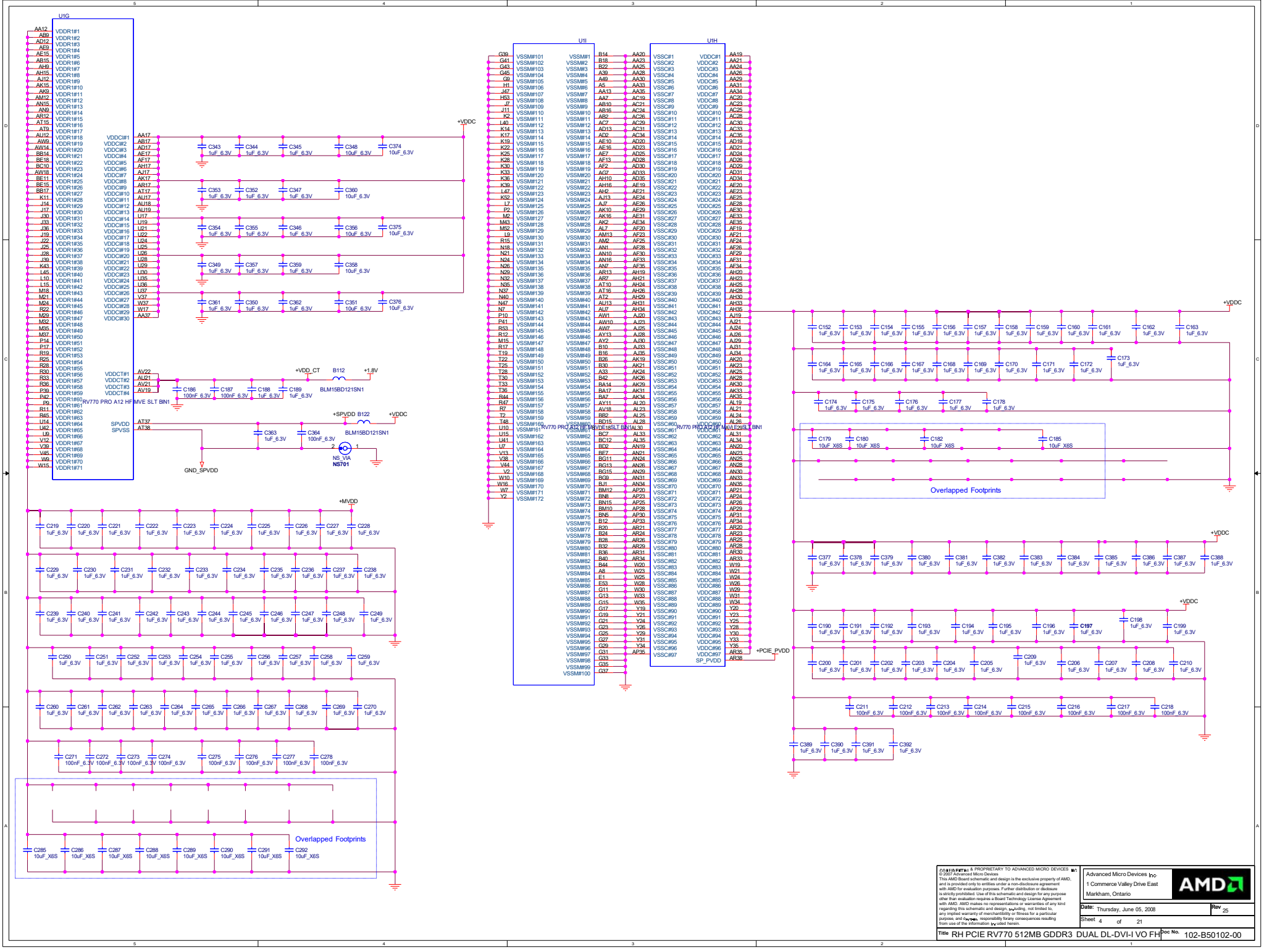
U1G
U1I
U1H
+VDDC
+MVDD
+PCIE_PVDD
+SPVDD
+VDD_CT
+1.8V
GND_SPVDD
BLM15BD121SN1
NS701
Overlapped Footprints
Overlapped Footprints
RV770 PRO A12 HF MVE SLT BIN1
RV770 PRO A12 HF MVE SLT BIN1
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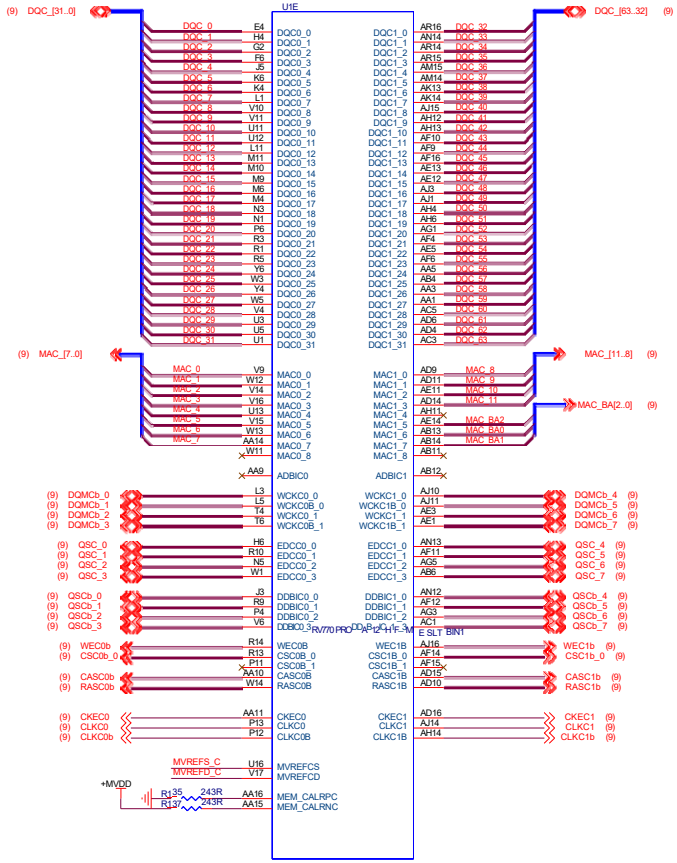
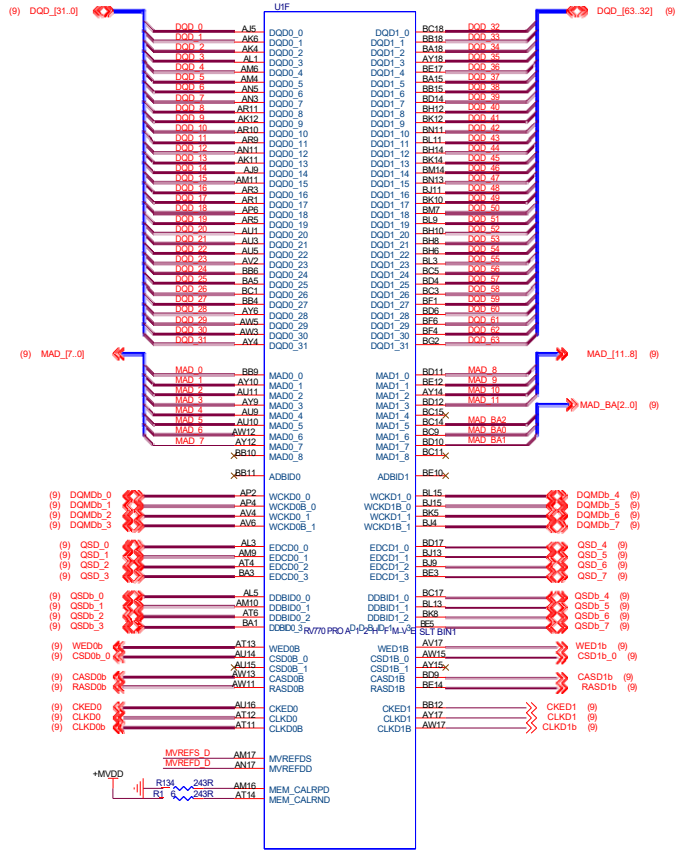
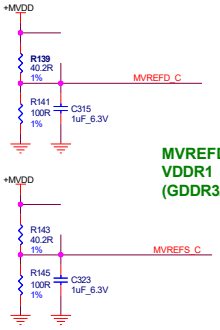
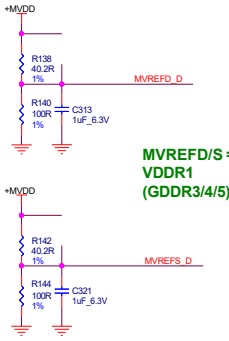






MVREFD/S =0.7*
VDDR1
(GDDR3/4/5)



MVREFD/S =0.7*
VDDR1
(GDDR3/4/5)

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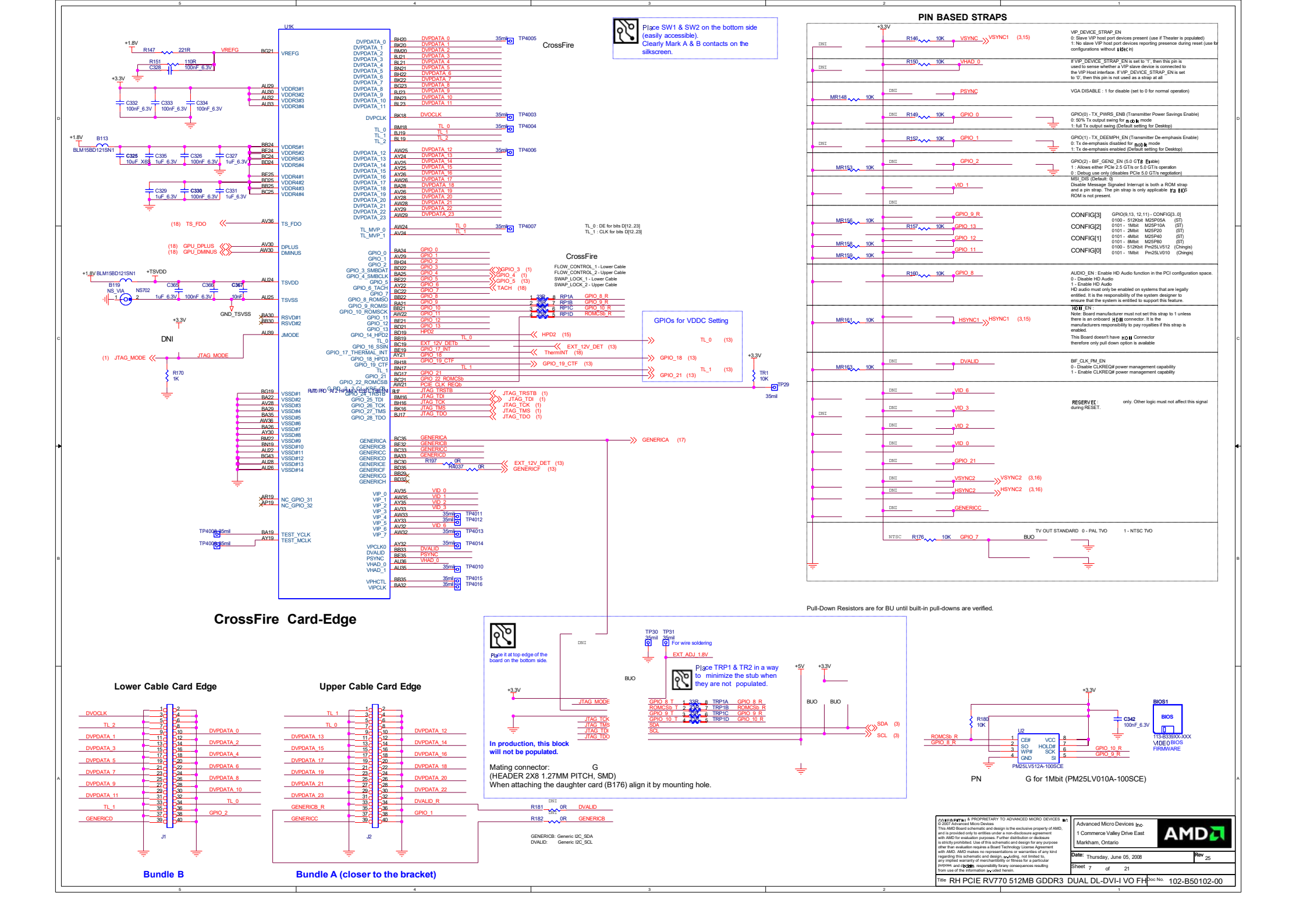
PIN BASED STRAPS
CrossFire Card-Edge
Lower Cable Card Edge
Upper Cable Card Edge
Bundle B
Bundle A (closer to the bracket)
Place SW1 & SW2 on the bottom side (easily accessible).
Clearly Mark A & B contacts on the silkscreen.
CrossFire
GPIOs for VDDC Setting
Pull-Down Resistors are for BU until built-in pull-downs are verified.
Place it at top edge of the board on the bottom side.
Place TRP1 & TR2 in a way to minimize the stub when they are not populated.
In production, this block will not be populated.
Mating connector: G
(HEADER 2X8 1.27MM PITCH, SMD)
When attaching the daughter card (B176) align it by mounting hole.
PN G for 1Mbit (PM25LV010A-100SCE)
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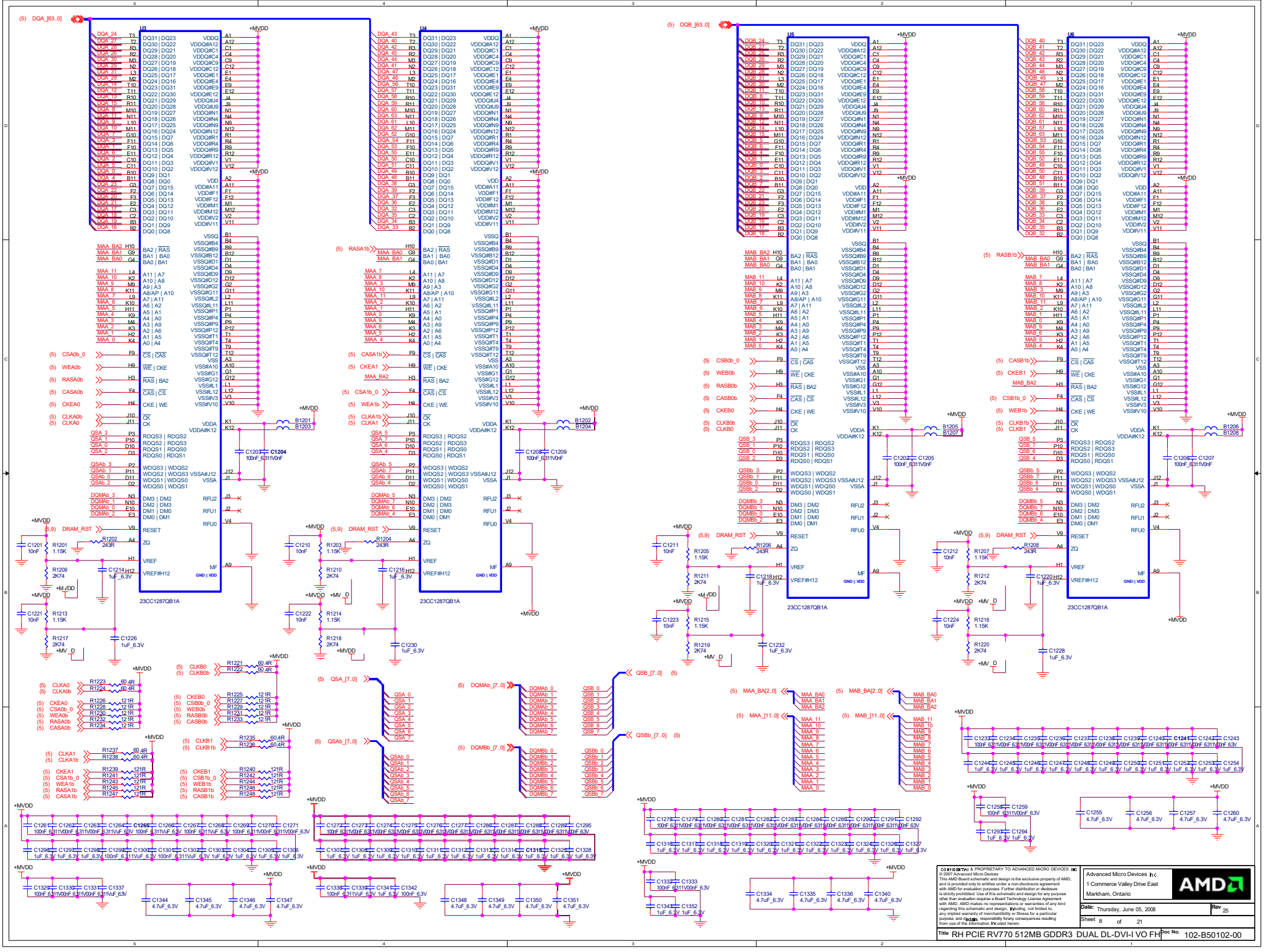
(5) DQA_[63..0]
(5) DQB_[63..0]
U3
U4
U5
U6
23CC1287QB1A
+MVDD
DRAM_RST
(5) CSA0b_0
(5) WEA0b
(5) RASA0b
(5) CASA0b
(5) CKEA0
(5) CLKA0b
(5) CLKA0
(5) RASA1b
(5) CASA1b
(5) CSA1b_0
(5) WEA1b
(5) CKEA1
(5) CLKA1b
(5) CLKA1
(5) CSB0b_0
(5) WEB0b
(5) RASB0b
(5) CASB0b
(5) CKEB0
(5) CLKB0b
(5) CLKB0
(5) CSB1b_0
(5) WEB1b
(5) RASB1b
(5) CASB1b
(5) CKEB1
(5) CLKB1b
(5) CLKB1
QSA_[7..0]
QSB_[7..0]
DQMAb_[7..0]
DQMBb_[7..0]
MAA_BA[2..0]
MAA_[11..0]
MAB_BA[2..0]
MAB_[11..0]
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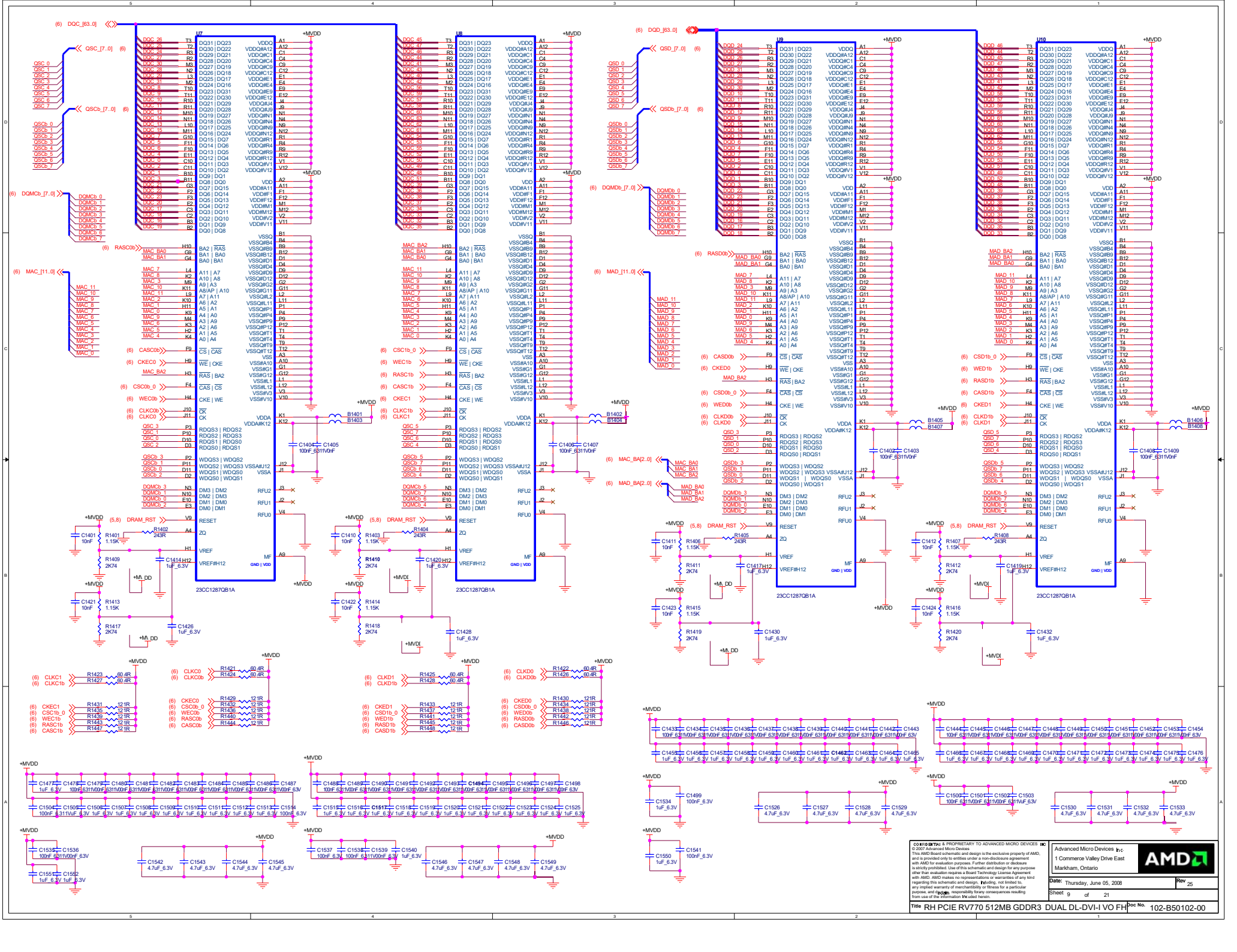

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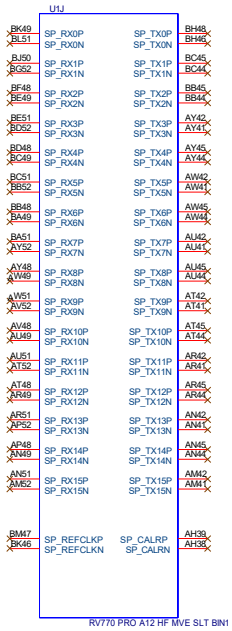

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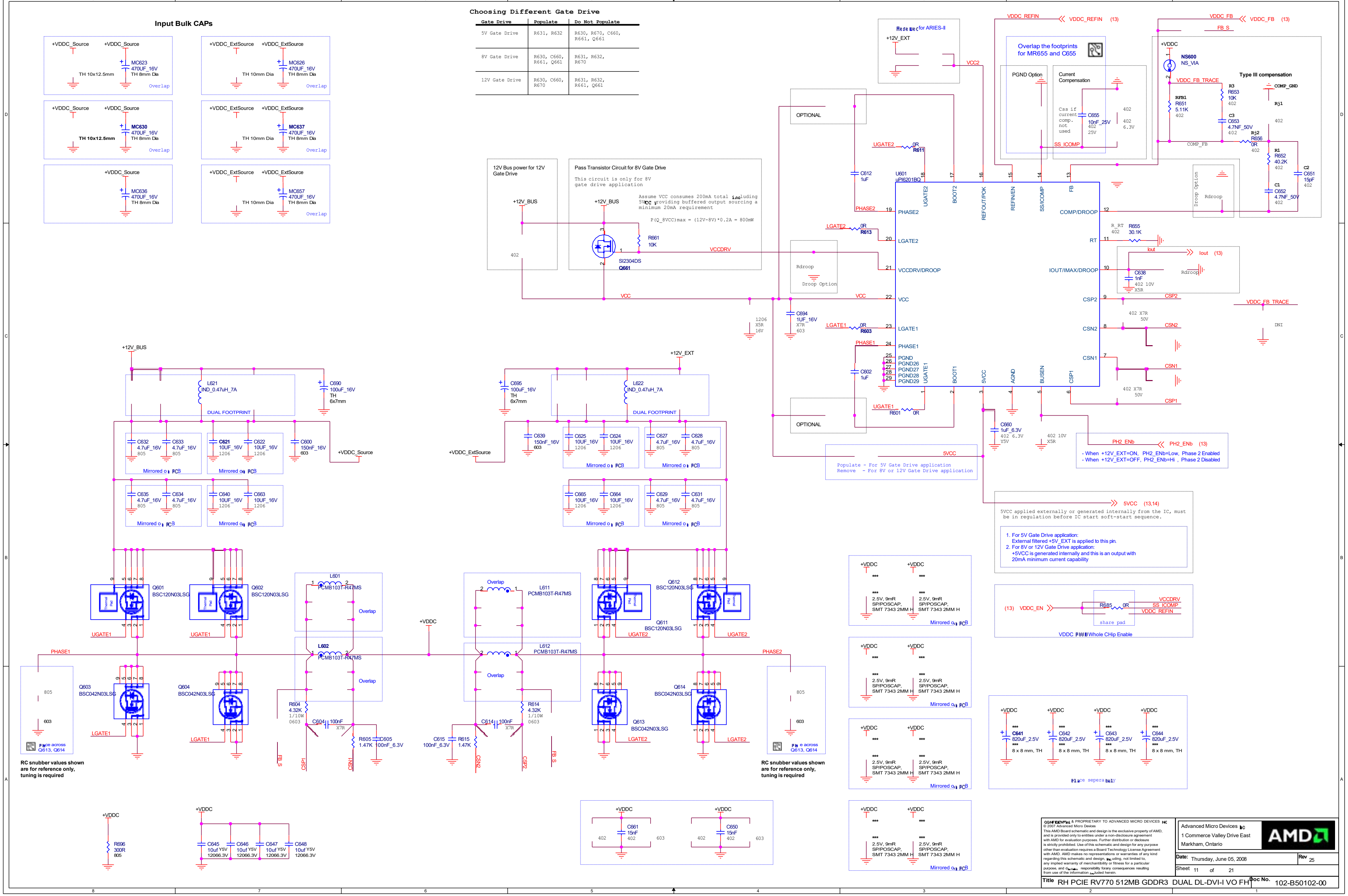

Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661

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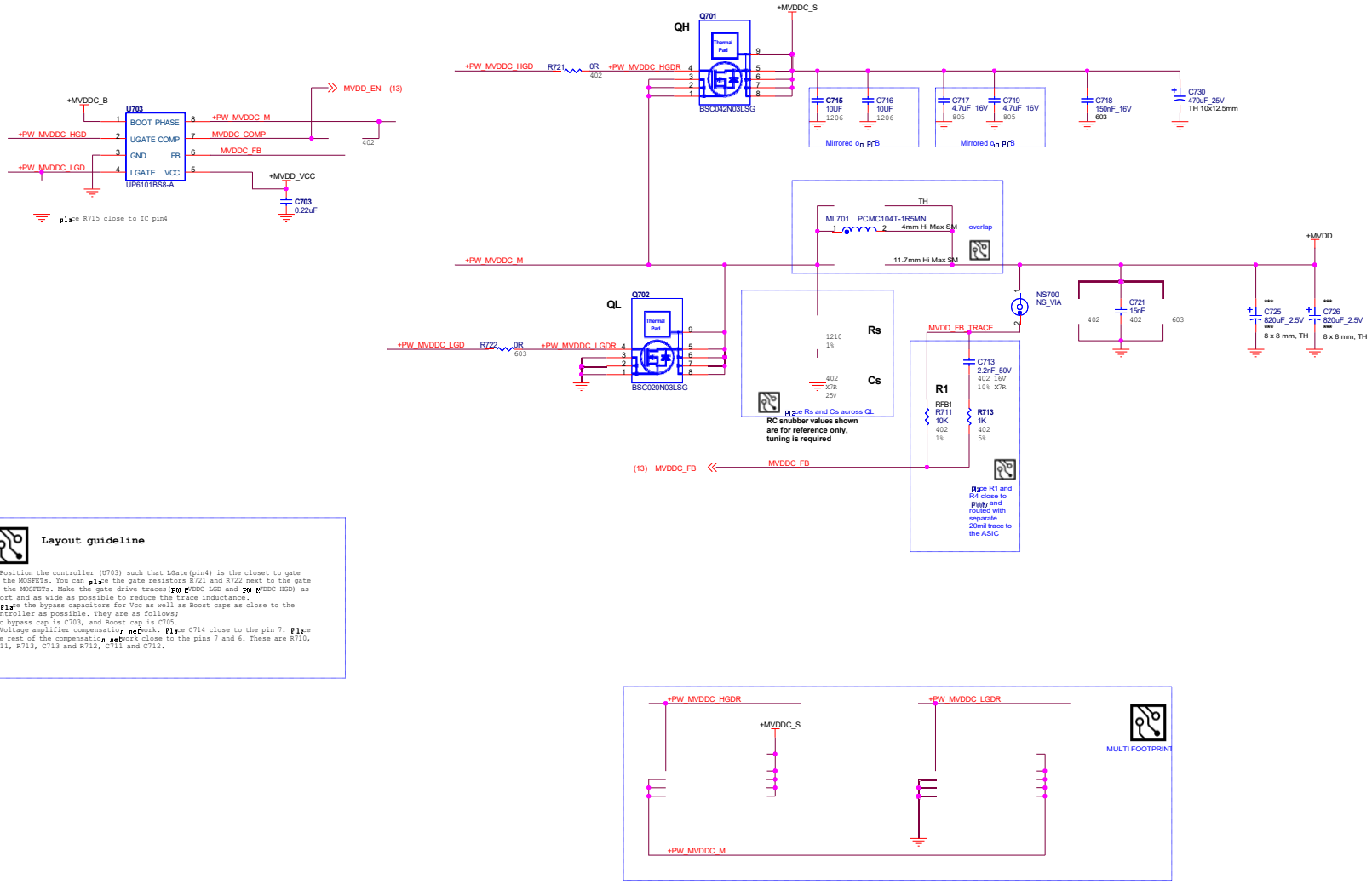
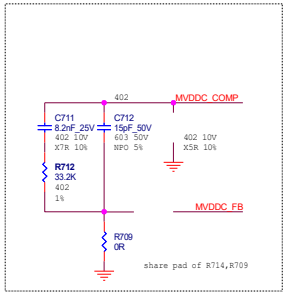


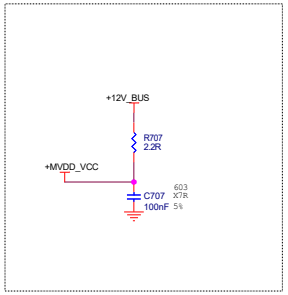
Layout guideline

1- Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces (pin MVDDC LGD and pin MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2- Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3- Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

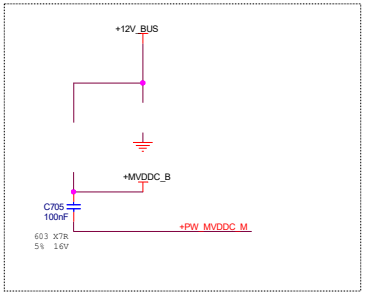
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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12V_EXT Connector

VDDC_EN is open collector and it is deactivated (pulled down to ground) when: EN_INTb =1 OR EN_Tb =1 OR (EN_EXTb =1 AND SENSE_GND_PIN=0)

Overlap MC1603 and C1603

Phase Control Support

4-bit VID for VDDC Setting

(bit 5 is fixed to zero VID4=0)

Place all parts close to the regulator that uses the voltage reference. R1673 & R1674 can be placed close to GPU for easy access to +3.3V.

R1687 & R1688 must be selected to limit MAX ref voltage to MAX VDDC.

See BOM for qualified values.

R636, R639 share pad

External Reference is used when REFIN is driven by voltage ranged from 0.4V to 3.3V

Internal Reference is used when REFIN is pull-up to > 4.5V

Table 4 VDDC Vref Mode Selection

Vref Mode	R636	R639/C659	Vref (V)
Internal	Populate	NC	0.6
External	NC	Populate	set by VID IC (U1220)

Power up Sequencing

AUX plug Enforcement option (BUO not for production)

12V AUX Power up Fault Support

12V/3.3V Bonding

AUX Hot Plug/ Unplug Fault supprt

Bypass Switch (not for production)

Red LED On, shows 12V AUX fault

Critical Temperature Support

Red LED On, shows critical temperature fault

Bypass Switch (not for production)

MVDD Input Option Circuit

VDDC Transient Test Circuit

For testing only, not intended for production

10x Buffered VDDC Output Current Monitoring

Temp Comp

For testing only, not intended for production

16-bit ADC for voltage & current read back

Install only R1270 or MR1270

Connect to +VDDC & +MVDD at the ASIC

For testing only, not intended for production

See BOM for qualified config.

Table 5 PTC Thermal Protection

PTC	THEM_PRT
>= Thermal shutdown temp (R>=4.7K)	Low
< Thermal shutdown temp (R < 4.7K)	Hi

- Place PTC1, PTC2 close to VDDC MOSFET
- Place PTC3, PTC4 close to MVDD

Table 2: VDDC Enable/Shutdown

EN_INTb asserted (0) when:	+12V_BUS & +3.3V_BUS are passed the threshold limit set by the voltage dividers
EN_EXTb asserted (0) when:	External cable plugged in, and +12V_EXT is passed the threshold limit set by the voltage divider
EN_Tb	This will be cleared at power-up, and will be set when Critical Temperature is reached
EXT_12V_DET (Active High)	On rising edge of LDO_EN, condition of PH2_EN is latched to determine the status of EXT cable.

VDDC Low Side Divider

R650 must be populated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.

- VDDC Hi-Side Divider R651 is Fixed to 5.11K
- Vo = Vref * (1 + R651 / R650)
- Vref = 0.6V

12V_BUS & 12V_EXT Input Switch Circuit

FDS6675, -10A, -30V, SO-8 (G)
Alt. FDS7779Z, -16A, -30V, SO-8 (G)
Put copper area under Q1230/1231 for heat dissipation.

Table 3

0: OFF / 1: ON			0: OFF / 1: ON		Status
12V_BUS	12V_EXT	EXT_12V_DET	Q1	Q2	
0	0	NA	NA	NA	No Power, No boot
1	0	0	1	1	Board is Powered by 12V_BUS, action taken by software
0	1	NA	0	0	No 12V_BUS, No boot
1	1	1	0	0	Boot up in normal condition

PTC Comparator Solution

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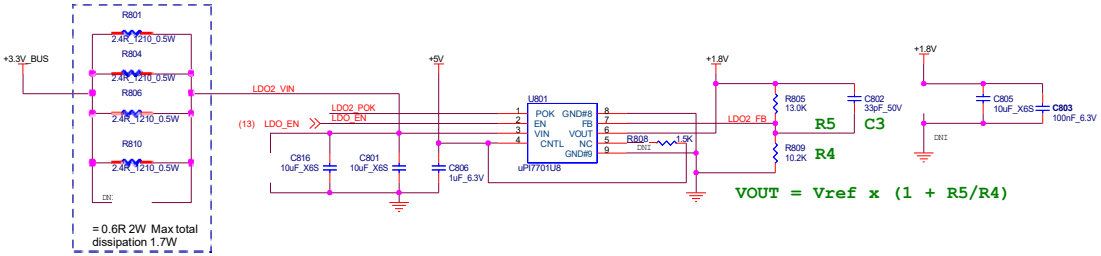
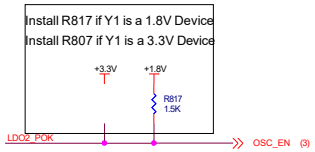
LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 1.7A (TBV) RMS MAX

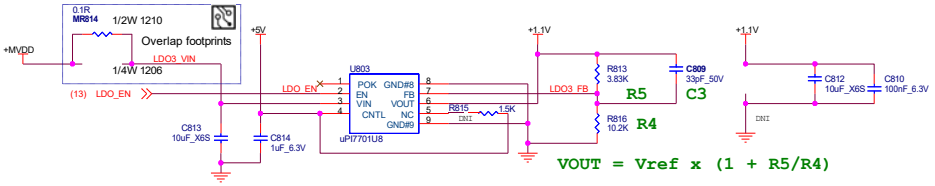
PCB: Min 70mm sq. copper area for cooling



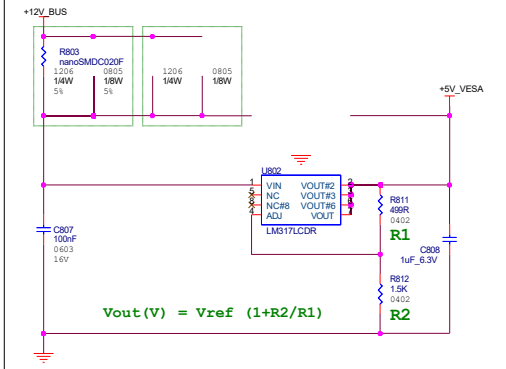


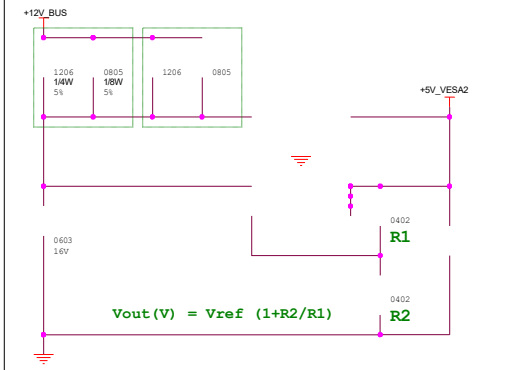
LDO #3: Vin = +1.50V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX

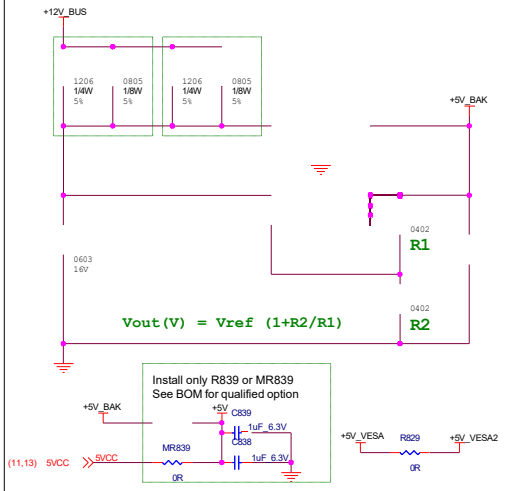
PCB: Min 70mm sq. copper area for cooling



Regulators for +5V, +5V_VESA and +5V_VESA2







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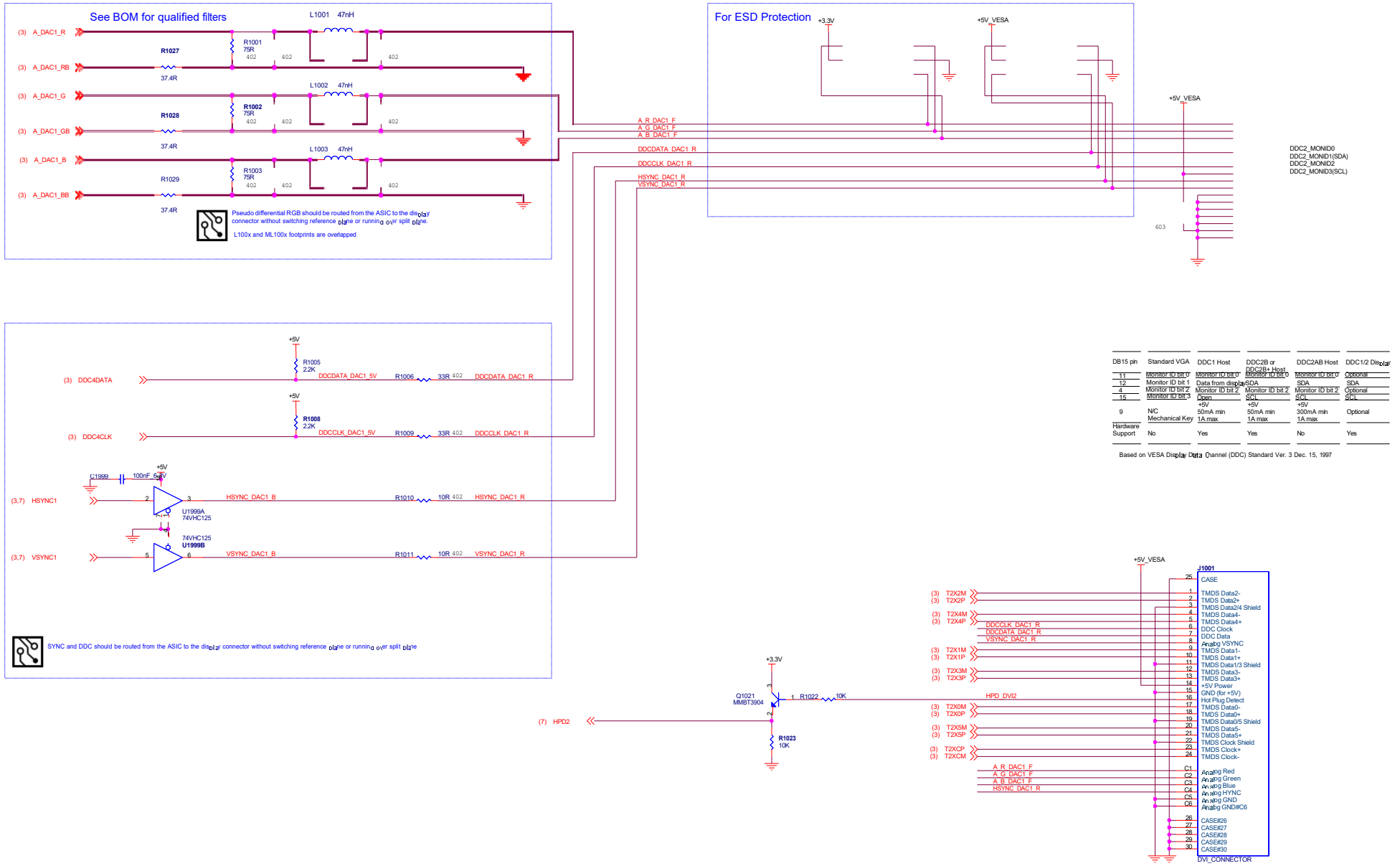

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	+5V Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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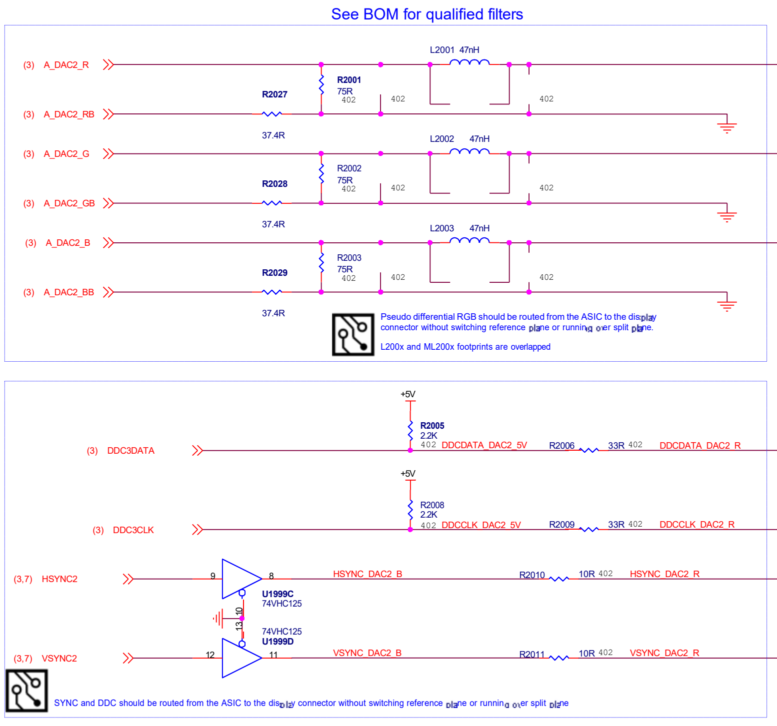
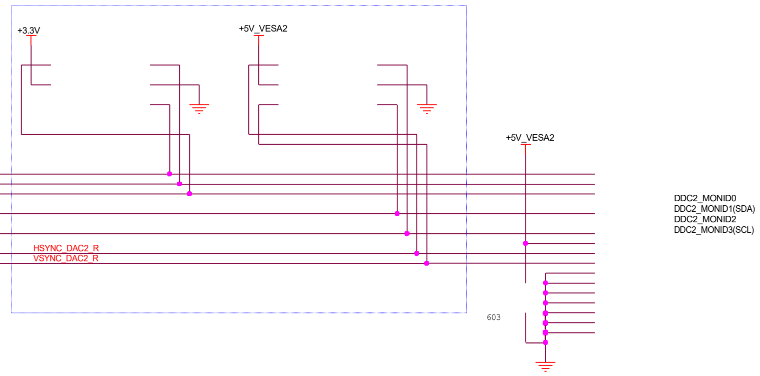
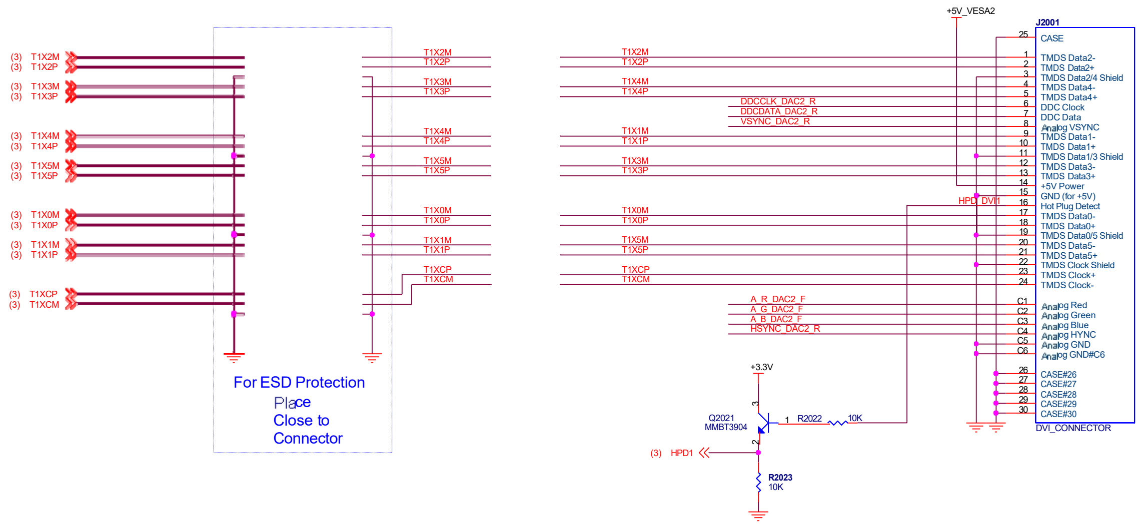




DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C Mechanical Key	+5V 50mA min 1A max	+5V 50mA min 1A max	+5V 300mA min 1A max	Optional
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997



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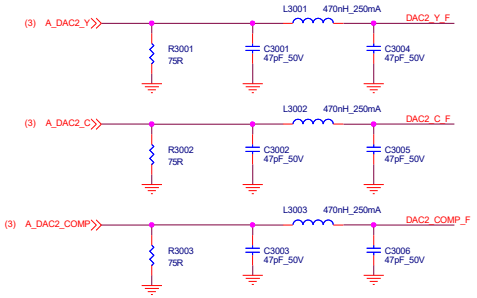

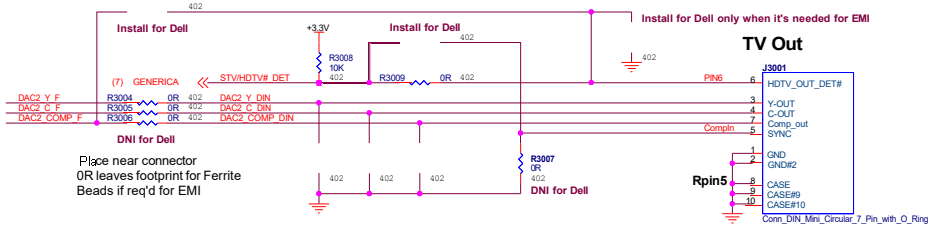

- 4-pin Svideo MiniDIN P/N G

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