

EVB Schematic For RockChip RK3308

RK_EVB_RK3308_DDR3P116SD4_V11

PMIC: Discrete
RAM: DDR3
ROM: eMMC/Nand/SPI Nor + TF card
Interface: ACODEC/I2S/PDM/SPDIF/LCDC/MAC



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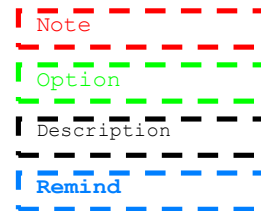
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Note

NOTE 1:
Component parameter description
 1. DNP stands for component not mounted temporarily
 2. If Value or option is DNP, which means the area is reserved without being mounted
 3. If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted

NOTE 2:
 Please use our recommended components to avoid too many changes.For more informations about the second source,please refer to our AVL.




Bill of Materials

Header:

Item\Part\Description\PCB Footprint\Reference\Quantity\Option


Combined property string:

{Item}\{Value}\{Description}\{PCB Footprint}\{Reference}\{Quantity}\{Option}

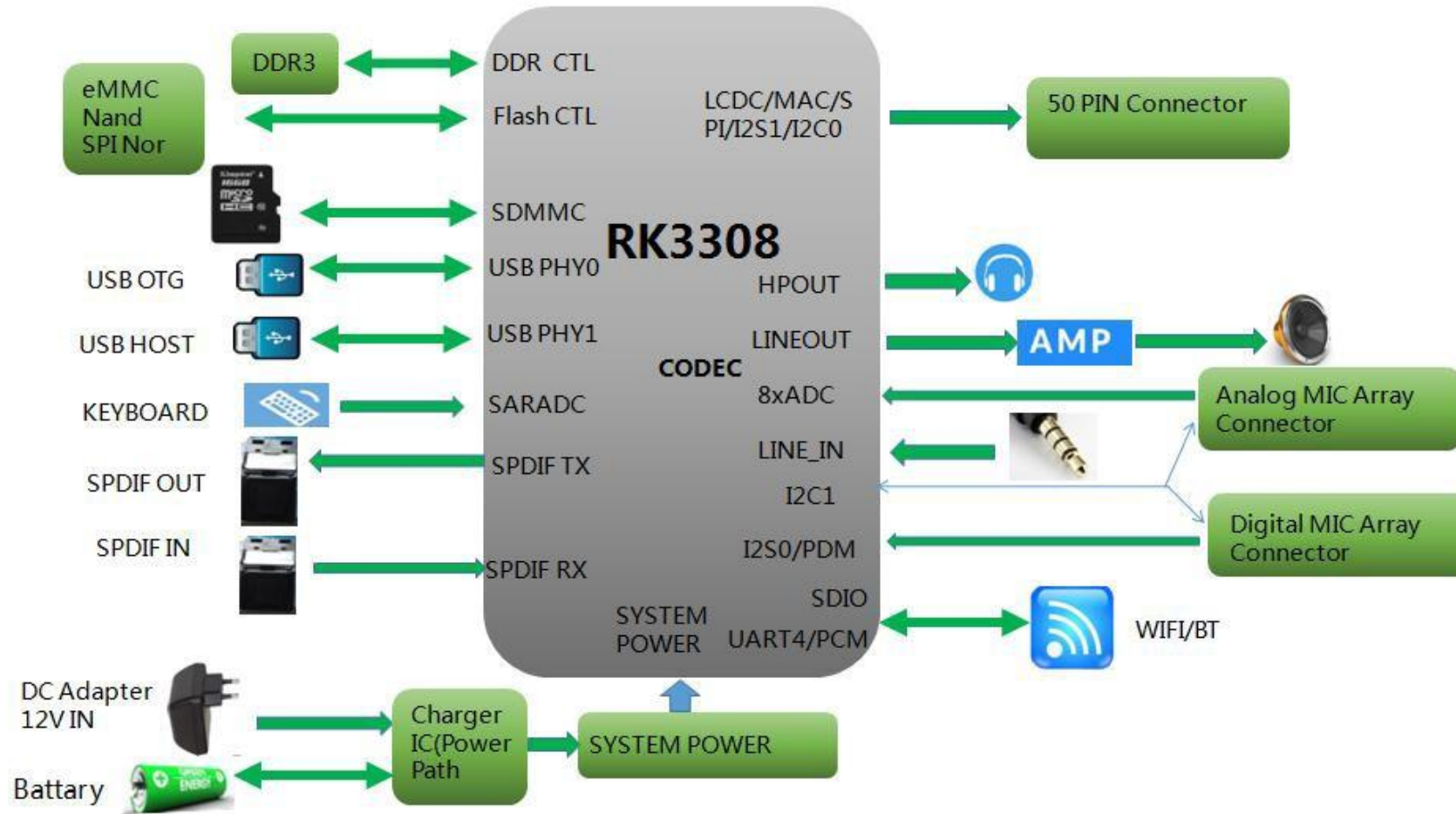
	
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Revision History

Version	Date	Author	Change Note	Approved
V1.0	2018.03.13	Joseph.Wei	First edition	
V1.1	2018.04.20	Joseph.Wei		

 Firefly		<hr/>	
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Block Diagram



	
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I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_D1/UART1_TX/I2C0_SCL/SPI2_CSN0 GPIO1_D0/UART1_RX/I2C0_SDA/SPI2_CLK	VCCIO1	I2C0_SCL I2C0_SDA	VCC_IO	Codec:ES8388	0X11	50 Pin Connector	
					G_Sensor	LIS3DH:0X19 MMA8452Q:0X1C	50 Pin Connector	
					LP_Sensor(TMD27723)	0x39	50 Pin Connector	
I2C1	GPIO0_B4/I2C1_SCL GPIO0_B3/I2C1_SDA	VCCIO0	I2C1_SCL I2C1_SDA	VCC_IO	SN3236	0x3C/0x3F	MIC Array Connector	
					ATSHA204A-SSHDA-T	0x64		
							Digital Array Connector	
I2C2	GPIO2_A3/UART0_RTSN/SPI0_CSN0/I2C2_SCL GPIO2_A2/UART0_CTSN/SPI0_CLK/I2C2_SDA	VCCIO2	I2C2_SCL I2C2_SDA	APIO2_VDD				
I2C3	GPIO0_C0/Pin3/I2C3_SCL_M0 GPIO0_B7/Pin2/I2C3_SDA_M0	VCCIO0	I2C3_SCL_M0 I2C3_SDA_M0	VCC_IO				
	GPIO3_B5/FLASH_CSN0/I2C3_SCL_M1/SPI1_CSN0/UART3_TX GPIO3_B4/FLASH_RDY/I2C3_SDA_M1/SPI1_MOSI/UART3_RX	VCCIO3	I2C3_SCL_M1 I2C3_SDA_M1	VCCIO_FLASH				



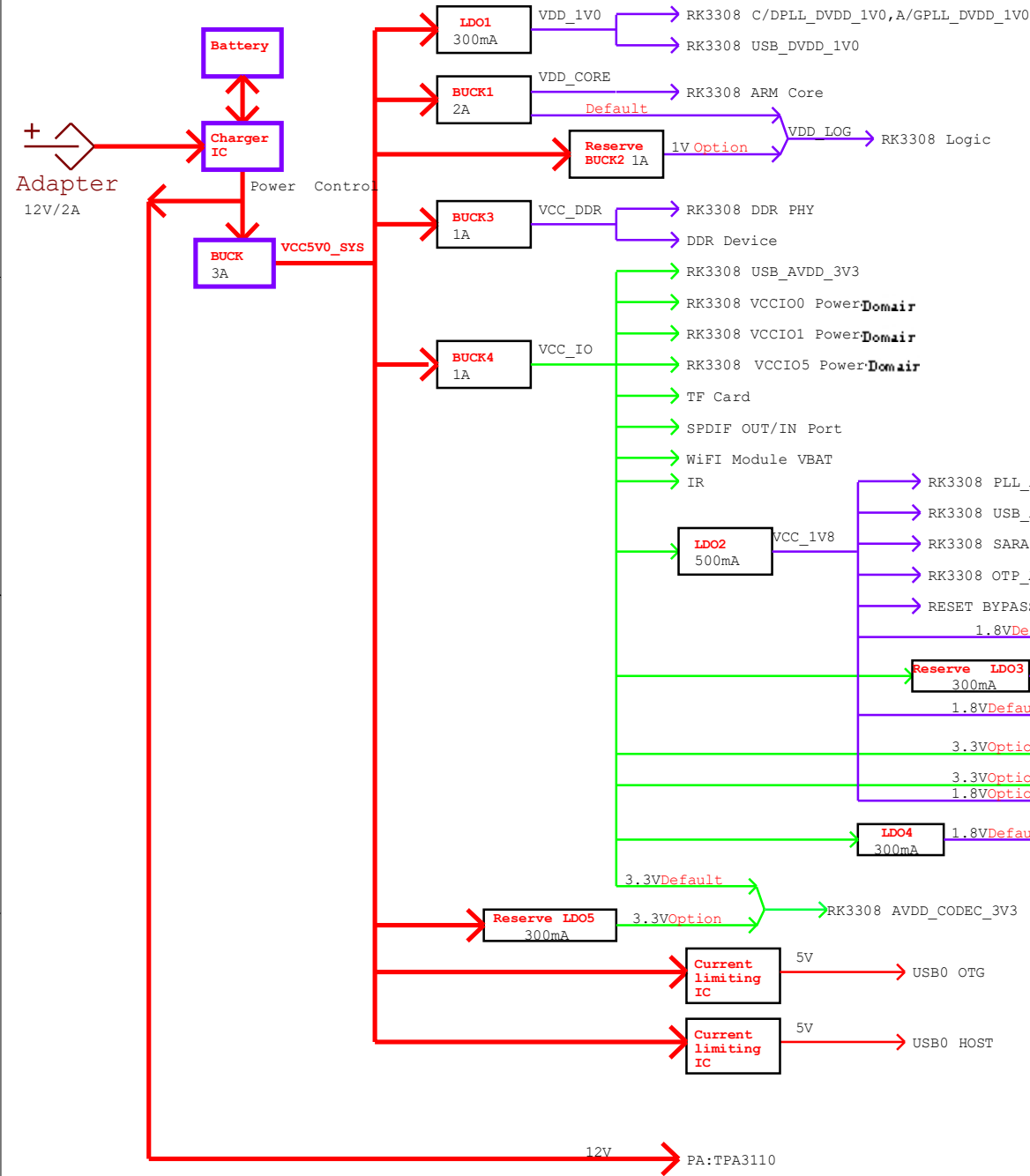
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Power Diagram and Sequence

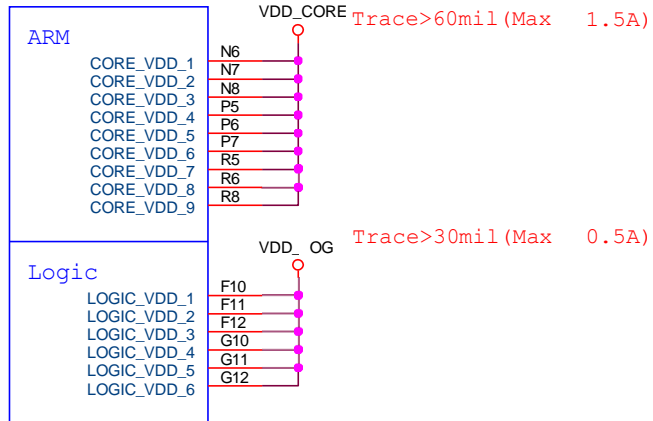


Power up Timing

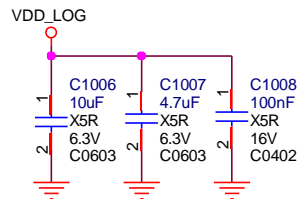
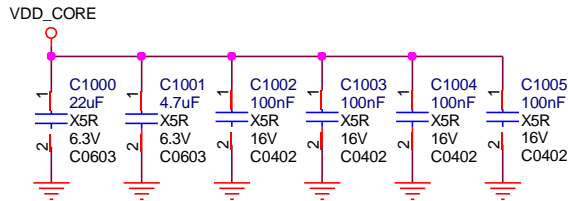
PowerName		timer	Default voltage	Normal voltage
VCC5V0_SYS	DCDC	Slot:1	5.0V	5.0V
VDD_LOG	DCDC	Slot:2	1.0V	1.0V
VDD_CORE	DCDC	Slot:2	1.0V	DVFS
VDD_1V0	LDO	Slot:2	1.0V	1.0V
VCC_DDR	DCDC	Slot:2	DDR3=1.5V DDR3L=1.35V	DDR3=1.5V DDR3L=1.35V
VCC_1V8	LDO	Slot:2	1.8V	1.8V
VCCIO_FLASH	LDO(1.8V) or VCC_IO	Slot:2	1.8V	1.8V or 3.3V
VCCIO_SDIO	LDO(1.8V) or VCC_IO	Slot:2	1.8V	1.8V or 3.3V
VCC_IO	DCDC	Slot:2	3.3V	3.3V
Reset		50mS		

IO PowerDomain	Voltage = 3.3V	Voltage = 1.8V
VCCIO0	3.3V (Default) PMUIO	Support
VCCIO1	3.3V (Default) LCDC	Support
VCCIO2	Support	1.8V (Default) I2S0
VCCIO3	Support	1.8V (Default) eMMC
VCCIO4	Support	1.8V (Default) WiFi (SDIO)
VCCIO5	3.3V (Default) SDMMC	Support

RK3308 Part-L

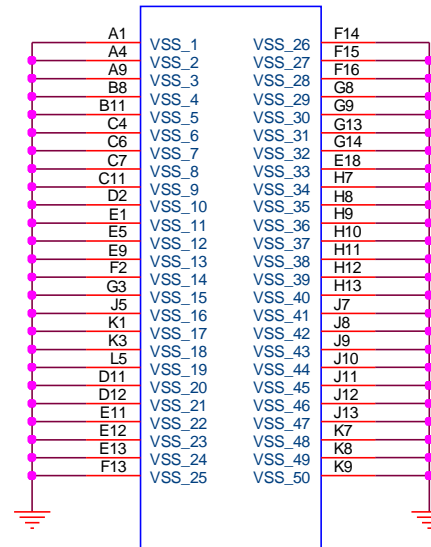


U1000L
RK3308_S
RK3308_S_BGA355_52R00X52R00X44R

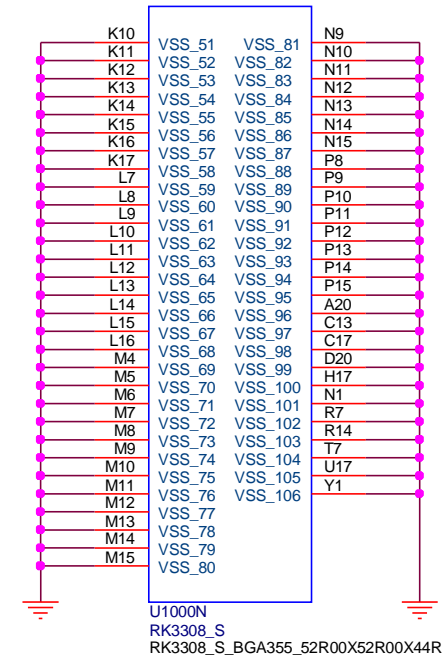


Note: All the Power filter capacitors should be placed close to the power pins of RK3308


RK3308 Part-N RK3308 Part-M



U1000M
RK3308_S
RK3308_S_BGA355_52R00X52R00X44R



U1000N
RK3308_S
RK3308_S_BGA355_52R00X52R00X44R



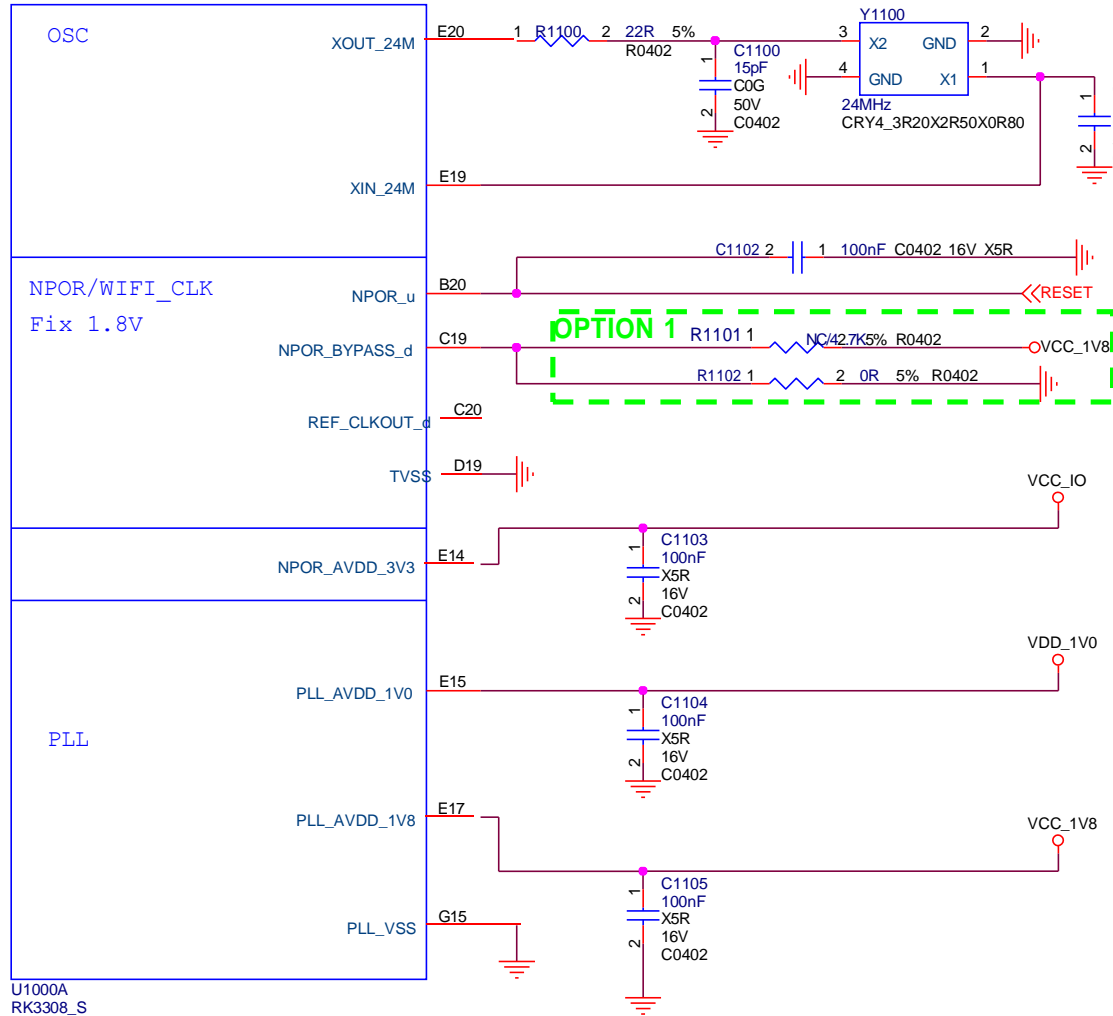
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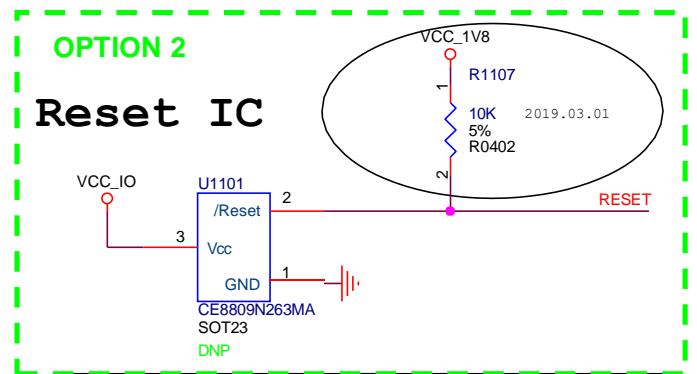
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RK3308 Part-A



If share clk source with WiFi,
Accuracy <= 10ppm.
Otherwise <=20ppm for
Independent crystal design



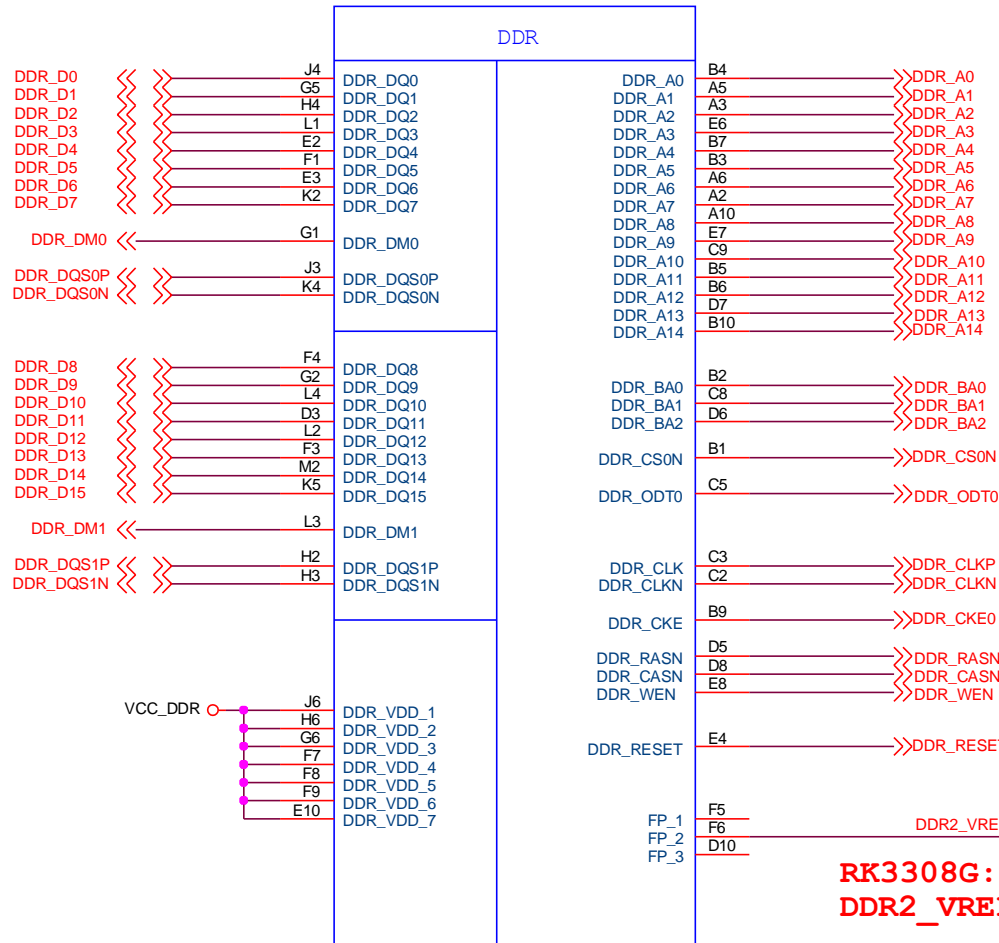
	Embedded Reset (Default)	External Reset
Option1	R1101=DNP R1102=0R	R1101=4.7K R1102=DNP
Option2	R1107=DNP U1101=DNP	R1107=10K U1101=Mounted

U1000A
RK3308_S
RK3308_S_BGA355_52R00X52R00X44R



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RK3308 Part-K



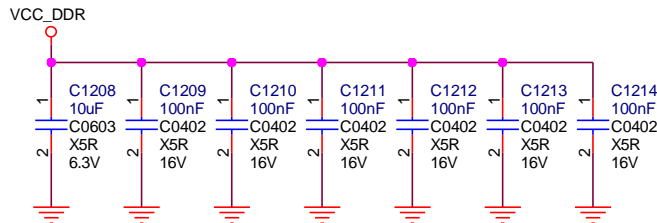
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RK3308_S
RK3308_S_BGA355_52R00X52R00X44R




**RK3308G:
DDR2_VREF**

**Note:
Reserver for RK3308G**

Power Filter

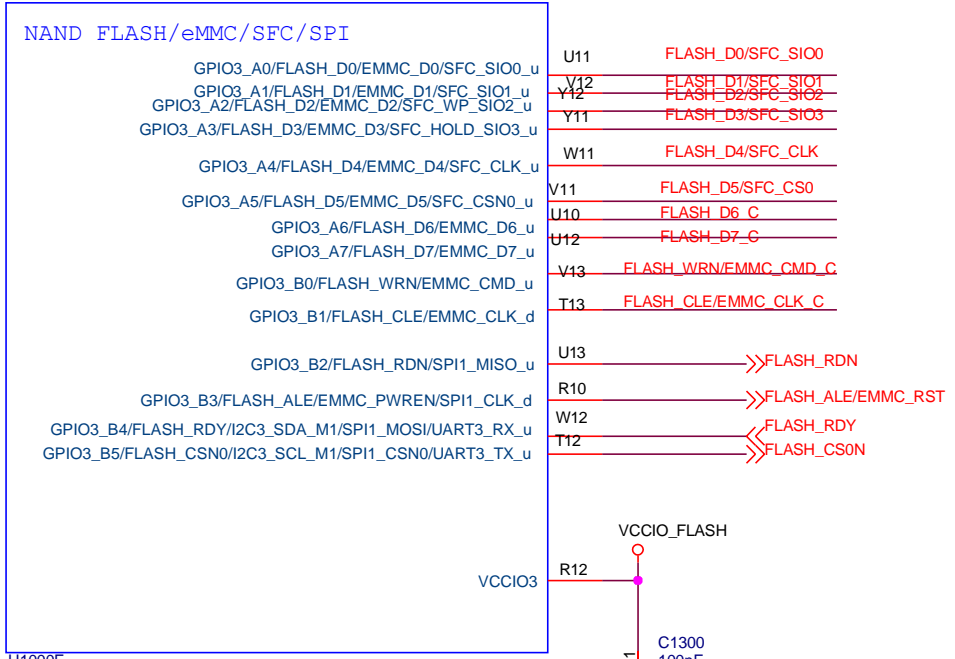


Note: All the Power filter capacitors should be placed close to the power pins of RK3308

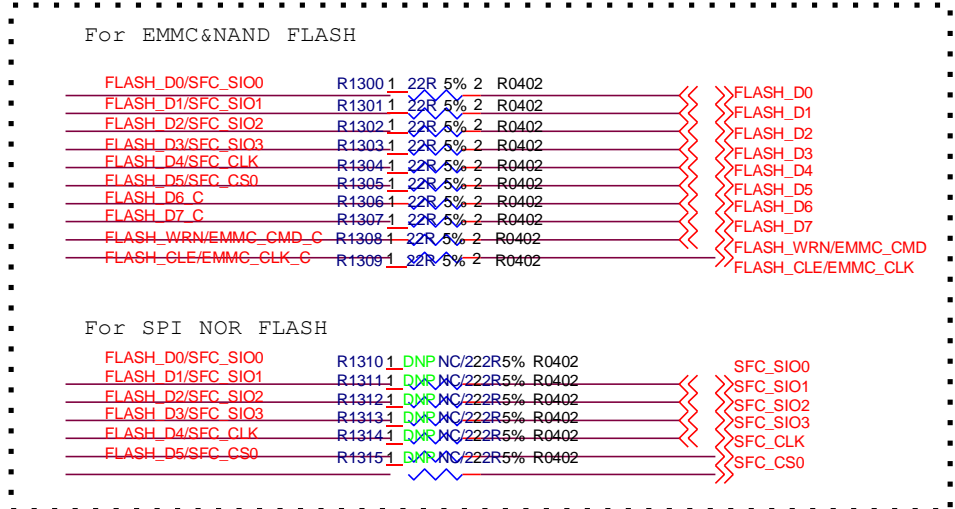
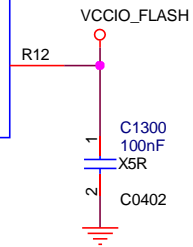



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RK3308 Part-E



U1000E
RK3308_S
RK3308_S_BGA355_52R00X52R00X44R

Firefly

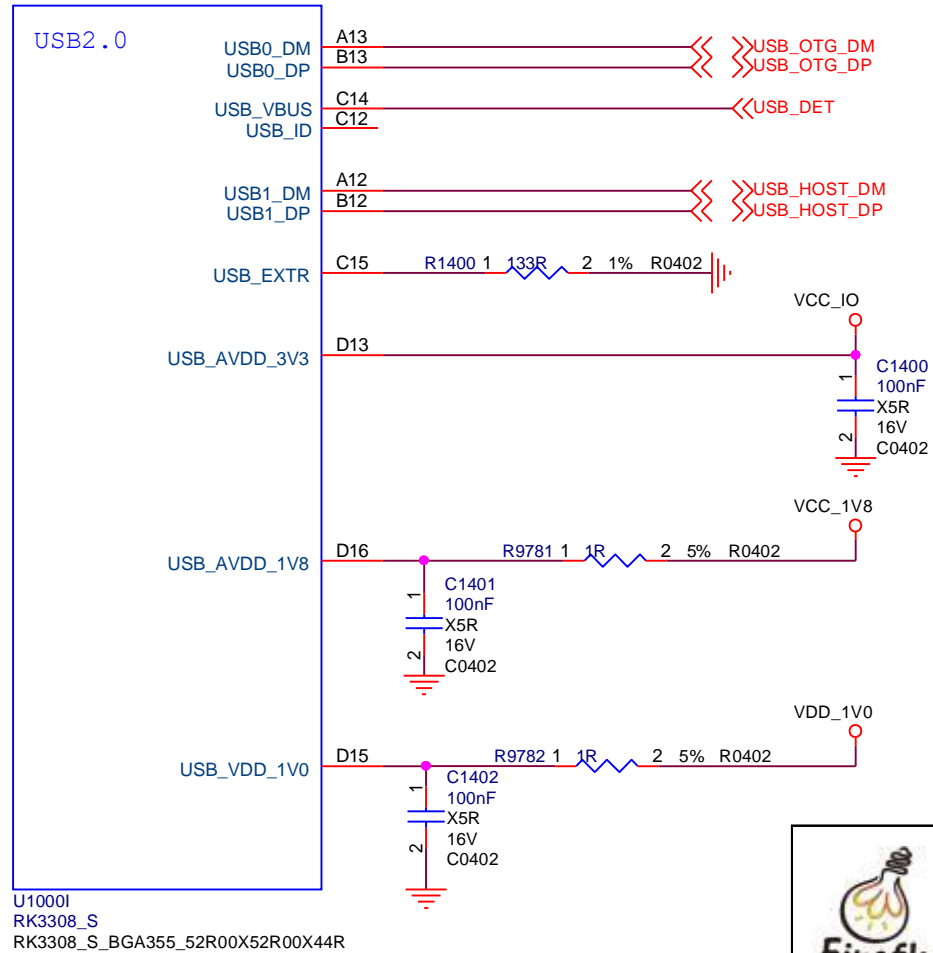

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RK3308 Part-I

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