PC8803
Automotive Single and Dual channel Antenna LDO with Current sensing

Overview

PC8803 features a high input voltage single low-dropout regulator (PC8803SC01 / PC8803SC03) / dual channel low-dropout regulator (PC8803SC02 / SC04) with accurate current sensing, designed to operate with a wide input voltage range from 4.5V to 40V. The device has 45V load dump protection at power input pin. These devices provide power to the low-noise amplifiers of the active antenna through a coaxial cable with 350mA per channel current. Each channel provides an adjustable output voltage from 1.5V to 20V through resistor divider on FB pin.

These devices provide diagnostics through the current sense and nERR pins. To monitor the load current, a high-side current sense circuitry provides a proportional analog output to the sensed load current. The accurate current sense allows detection of open, normal and short-circuit conditions without the need for further calibration. Current sense can be multiplexed between channels to save analog-to-digital converter (ADC) resources. Each channel also implements adjustable current limit with an external resistor on each LIM pin.

An integrated reverse polarity diode eliminates the need for an external diode. These devices feature standard thermal shutdown, short-to-battery protection on the output and reverse current protection. Each channel has internal inductive clamp protection on the output during the inductive switch off.

These devices operate over a -40°C to +125°C ambient temperature.
PC8803 is available in a 16-pin HTSSOP package.

Features

- Single and Dual channel LDO with current sense and adjustable current limit
- Wide input voltage range : 4.5V to 40V
- 45V Load dump
- Adjustable LDO VOUT : 1.5V to 20V
- Power load switch mode by shorting FB to GND
- Up to 350mA Output current
- Adjustable Current-Limit with external Resistor
- High Accuracy Current-Sense to Detect Antenna Open Condition at Low Current
- High PSRR : 80dB at 100Hz
- Reverse-Polarity protection, down to - 40V
- 500mV max dropout voltage at 100mA load
- Stabel with wide output capacitor, 2.2uF to 100uF (ESR 1mΩ to 5Ω)
- Integrated Protection and Diagnostics
  - ✓ Thermal Shutdown
  - ✓ Input Undervoltage Lockout (UVLO)
  - ✓ Short-Circuit Protection
  - ✓ Reverse Battery Polarity Protection
  - ✓ Reverse Current Protection
  - ✓ Output Short-to-Battery Protection
  - ✓ Output inductive Load Clamp
  - ✓ Ability to Distinguish All Faults with Current Sense pin
- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - ✓ Device Temperature Grade 1: - 40°C to 125°C Ambient Operating Temperature Range
  - ✓ Device HBM ESD Classification 2
  - ✓ Device CDM ESD Classification C4B
- 16-Pin HTSSOP PowerPAD package

Applications

- Infotainment Active-Antenna Power Supplies
- Surround-view Camera Power Supplies
- High-side power switch

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Simplified Application Diagram

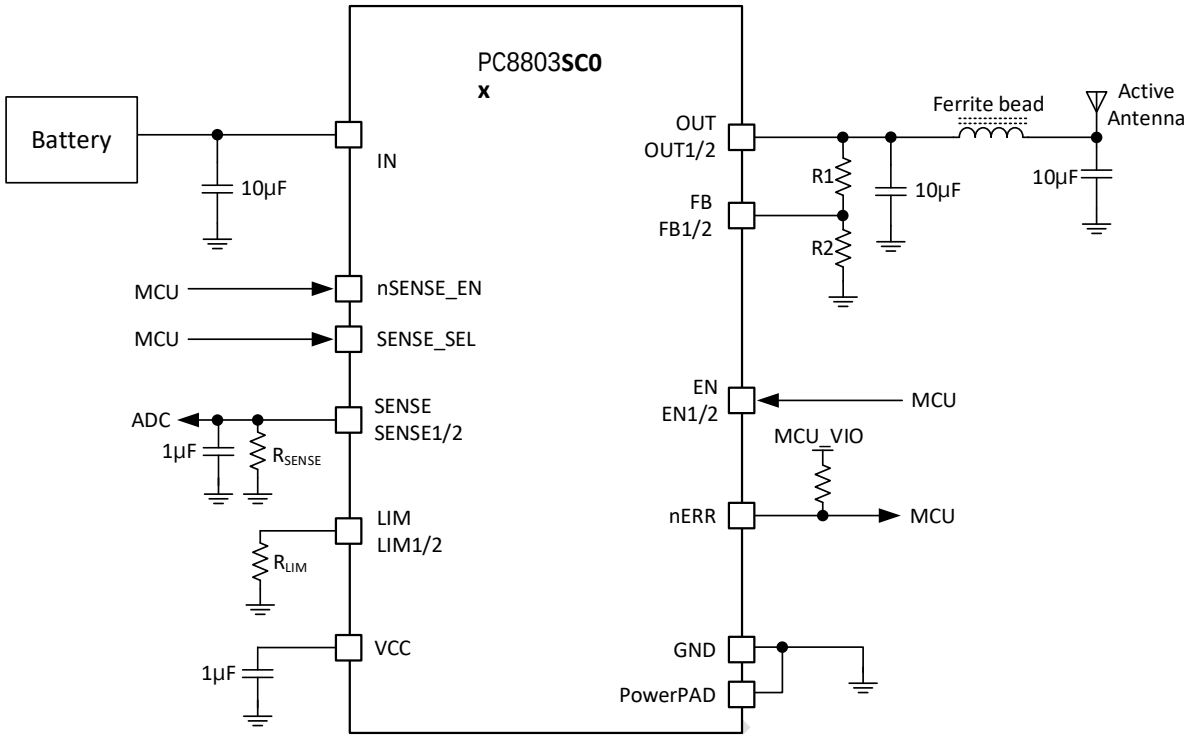

Figure 1. PC8803 application schematic

Ordering Information

Part Number	# of LDO	STB/RCP fault	Package	Op Temp
PC8803SC01Q1	Single	Latched OFF	HTSSOP, 16pin	-40 to 125°C
PC8803SC02Q1	Dual	Latched OFF	HTSSOP, 16pin	-40 to 125°C
PC8803SC03Q1	Single	Auto Retry	HTSSOP, 16pin	-40 to 125°C
PC8803SC04Q1	Dual	Auto Retry	HTSSOP, 16pin	-40 to 125°C

Pin Diagram

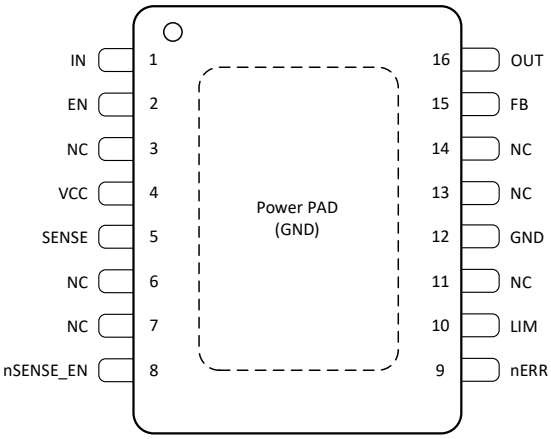

Figure 2. PC8803SC01/03 Pin Map

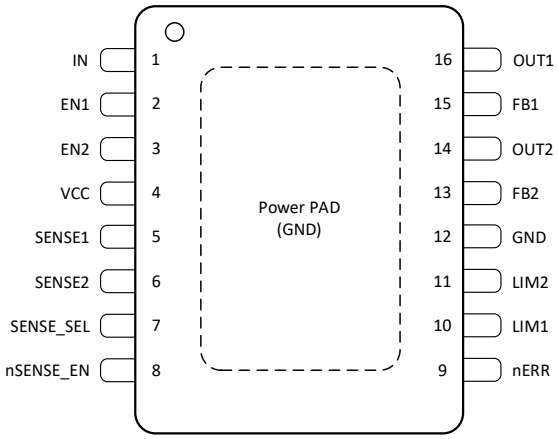

Figure 3. PC8803SC02/04 Pin Map

Pin Description

Table 1 Pin description
AI: Analog Input, AO: Analog Output, DI: Digital Input, DO: Digital Output, DIO: Digital Input and Output

Pin Name	PC8803 SC01/03	PC8803 SC02/04	Type	Description
IN	1	1	Power	Input Power supply voltage
EN	2	–	DI	Active high enable input for OUT pin
EN1	–	2	DI	Active high enable input for OUT1 pin
EN2	–	3	DI	Active high enable input for OUT2 pin
VCC	4	4	Power	Internal 4.5V regulator. Connect 1μF ceramic capacitor to GND
SENSE	5	–	AO	Output current sense for sensing. SENSE current is proportional to the current flow through OUT. To set the SENSE output voltage level, connect a resistor between this pin and GND. In addition, connect a 1μF capacitor from this pin to GND for frequency compensation of the current-sense loop. Short this pin to GND if not used.
SENSE1	–	5	AO	Output of current sense for sensing. SENSE1 current is proportional to the current flow through OUT1, and SENSE 2 current is proportional to OUT2 current when SENSE_SEL and SENSE_EN are low. To set the SENSEx output voltage level, connect a resistor between this pin and GND. In addition, connect a 1μF capacitor from the SENSEx pin to GND for frequency compensation of the current sense loop. Short the SENSEx pin to GND if not used.
SENSE2	–	6	AO	
SENSE_SEL	–	7	DI	This pin selects the current sense between channel 1 and channel 2. See Table TBD for details
nSENSE_EN	8	8	DI	Active low enable the current sense pin for multiplexing
nERR	9	9	DO	Open-drain fault indicator for general faults. External pull-up resistor is required
LIM	10	–	AI	Programmable current-limit pin. Connect a resistor to GND to set the current limitation level. To set to internal current limit, short this pin to GND.
LIM1	–	10	AI	Programmable OUT1 current-limit pin. Connect a resistor to GND to set the current limitation level. To set to internal current limit, short this pin to GND.

LIM2	–	11	AI	Programmable OUT2 current-limit pin. Connect a resistor to GND to set the current limitation level. To set to internal current limit, short this pin to GND.
GND	12	12	Power	Ground
FB	15	–	AI	Feedback input for setting OUT voltage. Connect FB to GND for current-limited switch operation.
FB1	–	15	AI	Feedback input for setting OUT1 voltage. Connect FB1 to GND for current-limited switch operation
FB2	–	13	AI	Feedback input for setting OUT2 voltage. Connect FB2 to GND for current-limited switch operation
OUT	16	–	Power	Output voltage
OUT1	–	16	Power	Output voltage 1
OUT2	–	14	Power	Output voltage 2
NC	3,6,11, 13,14	–	–	Internally not connected. Connect the NC pins to ground or leave floating.
	7	–	–	Internally connected. The pin must be either floated or connected to GND

Electrical Characteristics

Absolute Maximum Ratings (NOTE1)

Parameters	Pin		VALUE
Voltage range (with respect to GND unless specified)	IN		-40V ~ 45V
	OUT, OUT1, OUT2(NOTE2)		-0.3V ~ 45V
	EN, EN1, EN2		-0.3V ~ 45V
	VCC		-0.3V ~ 6V
	SENSE, SENSE1, SENSE2		-0.3V ~ VCC + 0.3V
	LIM, LIM1, LIM2		-0.3V ~ 7V
	FB, FB1, FB2		-0.3V ~ 7V
	SENSE_SEL, nSENSE_EN, nERR		-0.3V ~ 7V
Operating Junction temperature	T_J		-40°C to 150°C
Operating Ambient temperature	T_A		-40°C to 125°C
Storage temperature	$T_{STORAGE}$		-65°C to 150°C
ESD	HBM per AEC Q100-002		±2kV
	CDM per AEC Q100-011	Corner pins (1,8,9,16)	±750V
		Other pins	±500V

NOTE1: Stress beyond those listed under absolute maximum ratings may cause permanent damage to the device.
NOTE2: There is an internal diode connects between the OUT and GND pins for inductive clamp protection.

Recommended Operating Conditions (NOTE1)

Pin	Parameters	Min	Max	Unit
IN	Input voltage	4.5	40	V
EN, EN1, EN2	Enable input voltage	0	40	V
OUT, OUT1, OUT2	LDO mode	1.5	20	V
	Switch mode	4.5	35	V
FB, FB1, FB2		0	5.3	V
nSENSE_EN, SENSE_SEL, nERR, LIM, ILIM1, LIM2		0	5.3	V
SENSE, SENSE1, SENSE2		0	5.3	V
C_O	Output Capacitor stability range	2.2	100	μF
C_{O_ESR}	Output Capacitor ESR stability range	0.001	5	Ω
T_J	Operating Junction temperature	-40	150	°C
T_A	Operating Ambient temperature	-40	125	°C

NOTE1: Functional operation of the device at any other conditions beyond those indicated under recommended operating conditions are not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltage values are defined at ambient temperature range from -40°C to +125°C unless otherwise noted.

Thermal information

Parameters	Thermal Metric	PC8803SC01/03	PC8803SC02/04	Unit
$R_{\theta JA}$	Junction to Ambient thermal resistance (NOTE1)	45.9	40.3	°C/W
$R_{\theta JC}$	Junction to Case thermal resistance	29.2	27.7	°C/W
$R_{\theta JB}$	Junction to Board thermal resistance	24.7	22.3	°C/W

NOTE1 : The thermal data is based on JEDEC standard high K profile – JESD 51-7. The copper pad is soldered to the thermal land pattern.

Electrical Characteristics

V_{IN}=14V, C_{IN} = 10 µF, C_{OUT}=10µF, T_J = -40°C ~ 150°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power Supplies						
V_{IN}	VIN operating voltage		4.5		40	V
I_Q	Quiescent Current at GND	VIN = 4.5V to 40V, EN ≥ 2V, IOUT = 0.1mA (PC8803SC01/03)		0.6	1	mA
		VIN = 4.5V to 40V, EN1/EN2 ≥ 2V, IOUT1/IOUT2= 0.1mA (PC8803SC02/04)		0.6	1	mA
I_{SD}	Shutdown current	VIN = 14V, EN =0V (PC8803SC01/03)			10	µA
		VIN = 14V, EN1/EN2 =0V (PC8803SC02/04)			10	µA
I_{NOM_GND}	Operating current	EN ≥ 2V, IOUT ≤ 350mA, GND current (PC8803SC01/03)			4.5	mA
		EN1/EN2 ≥ 2V, IOUT1/IOUT2 ≤ 350mA, GND current (PC8803SC02/04)			6	mA
V_{IN_UVLO}	VIN UVLO Threshold	Falling	3.6	3.8	4.0	V
$V_{IN\_UVLO\_HYS}$	VIN UVLO Threshold Hysteresis			400		mV
V_{BG}	Bandgap voltage	Reference voltage of FB		1.233		V
V_{BG_ACC}	Bandgap voltage accuracy		-2		+2	%
Logic Output (nERR)						
V_{OL}	Output Logic Low voltage	I_{OL}=5mA			0.4	V
I_{LK}	Leakage Current	Output Hi-Z, pull up to 5V			1	µA
Logic Input (EN, EN1, EN2, nSENSE_EN, SENSE_SEL)						
V_{IH}	Logic input high voltage		2.0			V
V_{IL}	Logic input low voltage				0.7	V
$I_{LK\_nSENSE\_EN}$	Leakage Current	nSENSE_EN = 5V, VENx ≥ 2V			10	µA
$I_{LK\_SENSE\_SEL}$	Leakage Current	SENSE_SEL = 5V, VENx ≥ 2V			10	µA
I_{LK_EN}	Leakage Current	VENx = 40V			10	µA
REGULATED OUTPUT (OUT, OUT1, OUT2)						
V_{OUT_ACC}	Output Voltage Accuracy	IN > max(V_{OUT} + 1.5V, 4.5V), I_{OUT} = 1mA to 350mA	-2	0	+2	%
$\Delta V_{OUT\_\Delta IN}$	Line Regulation	IN = max(V_{OUT} +1.5V, 6V) to 40V, I_{OUT} = 10mA, FB voltage variation			10	mV
$\Delta V_{OUT\_\Delta IOUT}$	Load Regulation	I_{OUT} = 1mA to 200mA, FB voltage variation			20	mV
V_{DO}	Dropout voltage	I_{OUT} = 100mA			500	mV
I_{OUT}	Output Current		0		350	mA
PSRR	Power Supply Rejection Ratio			80		dB
R_{PD_OUT}	OUT Pull-down resistor	ENx = GND		50		KΩ
CURRENT SENSE and CURRENT LIMIT						
I_{SNS_RATIO}	Current sense Ratio	I_{OUT}/I_{SENSE}, I_{OUT} = 1mA to 350mA		198		

I_{SNS_ACC}	Current Sense accuracy	I_{OUT} = 100mA ~ 350mA	-3		+3	%
		I_{OUT} = 50mA ~ 100mA	-5		+5	%
		I_{OUT} = 10mA ~ 50mA	-10		+10	%
		I_{OUT} = 5mA ~ 10mA	-20		+20	%
I_{LIM_RATIO}	I_{LIM} Current Ratio	I_{OUT}/I_{LIM}, Limit current = 50mA ~ 350mA		198		
I_{LIM_ACC}	Current Limit Accuracy	Limit current = 50mA ~ 350mA	-8		8	%
I_{LIM_INT}	Internal Current limit	LIMx pin shorted to GND	360		550	mA
I_{LKG}	Leakage current	SENSE, SENSE1, SENSE2, LIM, LIM1, LIM2, ENx = GND, T_A = 25°C			2	µA
V_{LIM_TH}	Current limit threshold voltage	The voltage on LIM, LIM1, LIM2 during current limit		1.233		V
V_{SENSE_STB}	SENSE voltage at Short-to-Battery fault condition	When short-to-battery or reverse current conditions are detected	3.05	3.2	3.3	V
V_{SENSE_TSD}	SENSE voltage at thermal shutdown fault condition	When thermal shutdown is detected	2.7	2.85	3	V
V_{SENSE_CL}	SENSE voltage at current limit fault condition	When current-limit condition is detected	2.4	2.55	2.65	V
I_{SENSE_H}	SENSE current at fault condition	When short-to-battery, reverse current, thermal shutdown or current limit conditions are met	3.3			mA
FAULT DETECTION						
V_{STB_TH}	Short-to-battery threshold	$V_{OUT} – V_{IN}$, Check during turn on sequence	-500	-55	110	mV
I_{REV}	Reverse current detection level		-100	-40	-1	mA
T_{SD}	Thermal Shutdown	Rising Junction temperature		175		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			15		°C
VCC Regulator						
VCC	Internal voltage regulator	IN = 5.5 to 40V, I_{VCC} = 0mA	4.25	4.5	4.75	V
I_{VCC_LIM}	VCC current limit		15		70	mA
Timing spec						
$t_{d\_SENSE\_SEL\_R}$	SENSE_SEL delay time	EN = 5V, nSENSE_EN = 0V, SENSE_SEL = 0V to 5V		10		µs
$t_{d\_SENSE\_SEL\_F}$	SENSE_SEL delay time	EN = 5V, nSENSE_EN = 0V, SENSE_SEL = 5V to 0V		10		µs
$t_{d\_SENSE\_EN\_R}$	SENSE_EN delay time	EN = 5V, nSENSE_EN = 0V to 5V		10		µs
$t_{d\_SENSE\_EN\_F}$	SENSE_EN delay time	EN = 5V, nSENSE_EN = 5V to 0V		10		µs
t_{DEG_RC}	Reverse current(Short-to-Battery) deglitch time	LDO off after I_{OUT} = -200mA, T_A = 25°C		5	20	µs
t_{BLK_RC}	Reverse current blanking time	Blanking time for reverse-current detection after power up, the rising edge of the ENx pin, or the current limiting event is over		16		ms

Typical Operating Characteristics

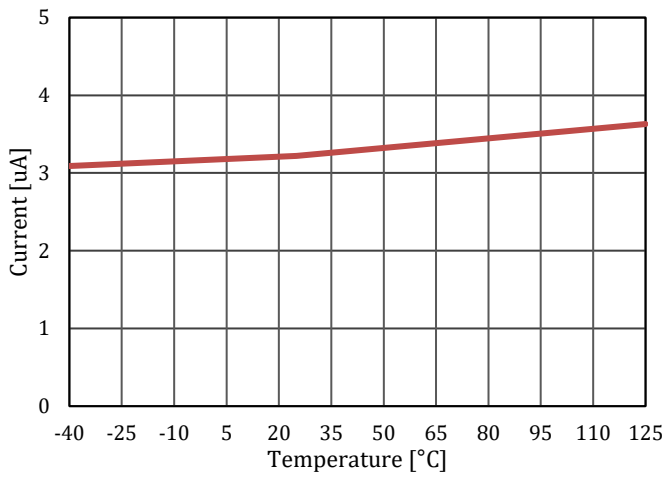

Figure 4 Shutdown current

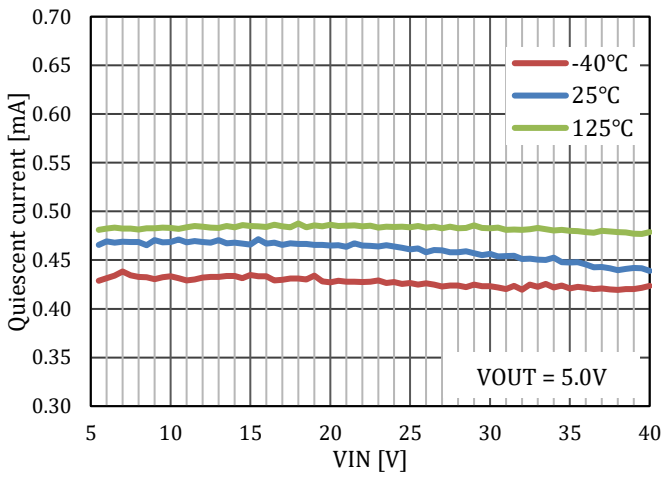

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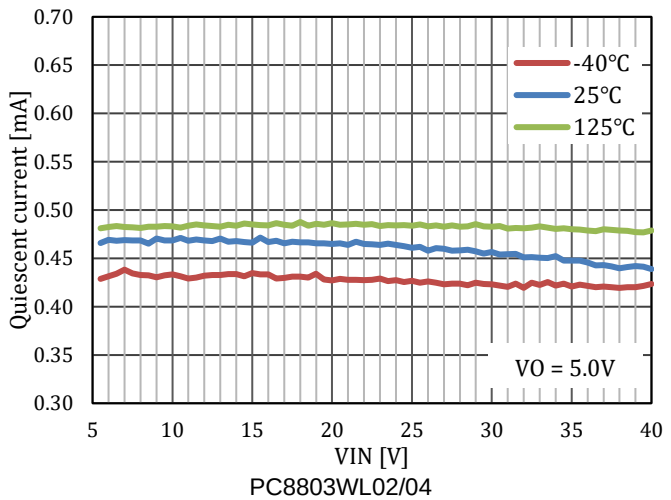
Figure 5 Quiescent GND current



PC8803WL02/04

Figure 6 Quiescent GND Current

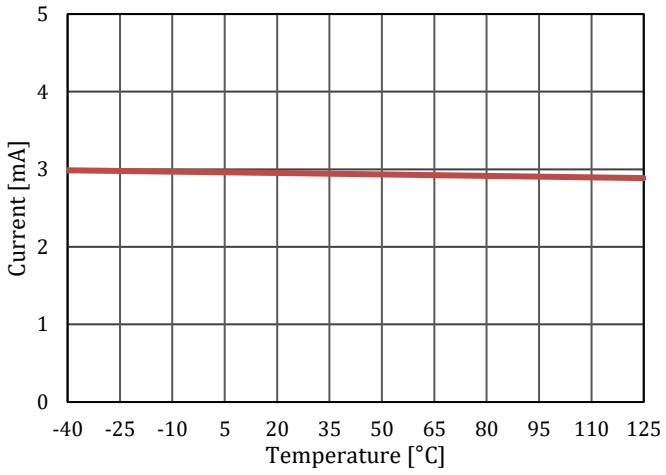
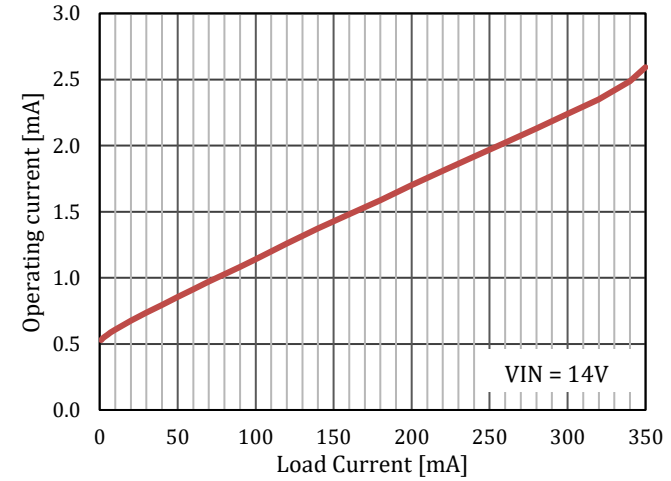
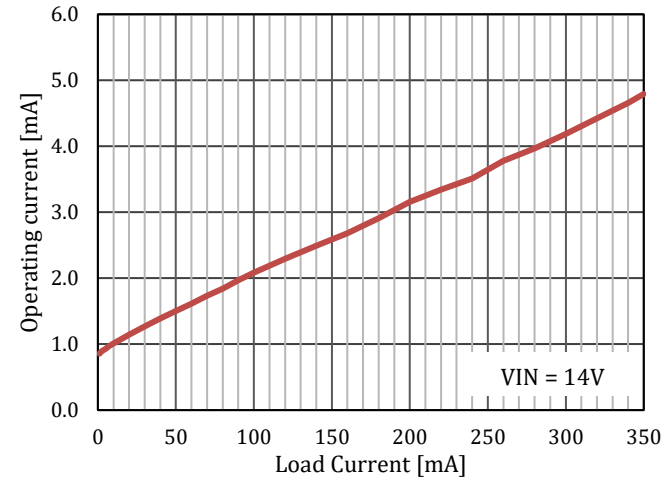


Figure 7 Quiescent current in SW mode



PC8803WL01/03

Figure 8 Operating GND Current



PC8803WL02/04

Figure 9 Operating GND Current

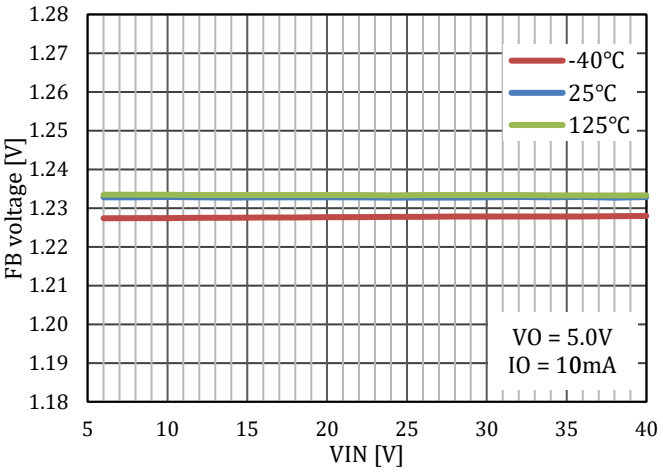


Figure 10 FB voltage Vs VIN

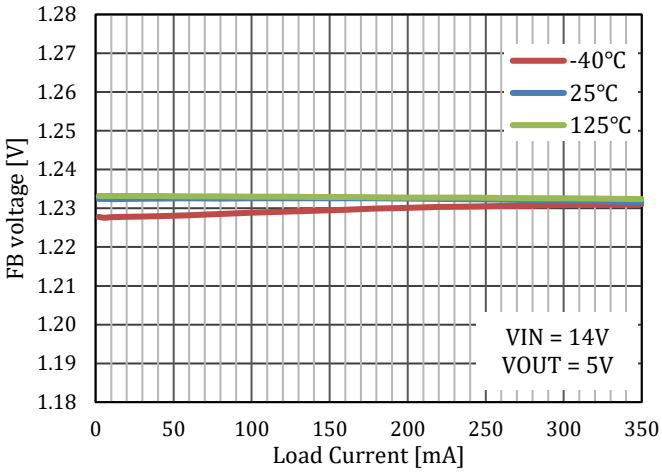


Figure 11 FB voltage Vs Output current

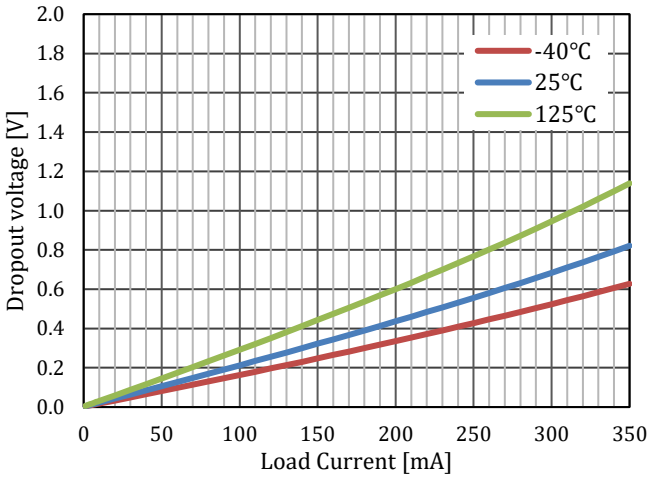


Figure 12 LDO1 Dropout voltage

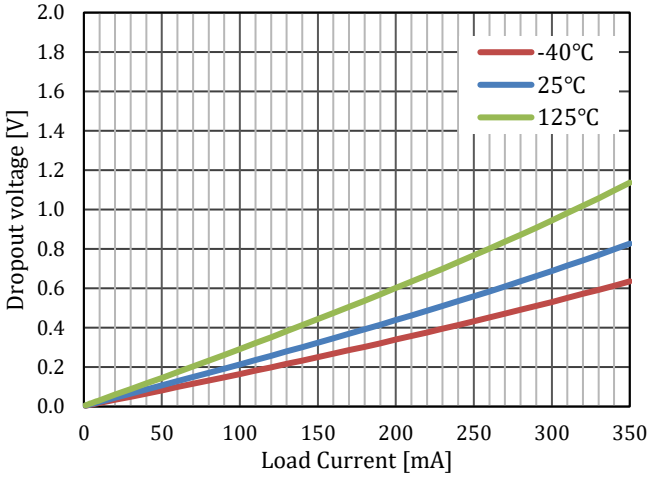


Figure 13 LDO2 Dropout voltage

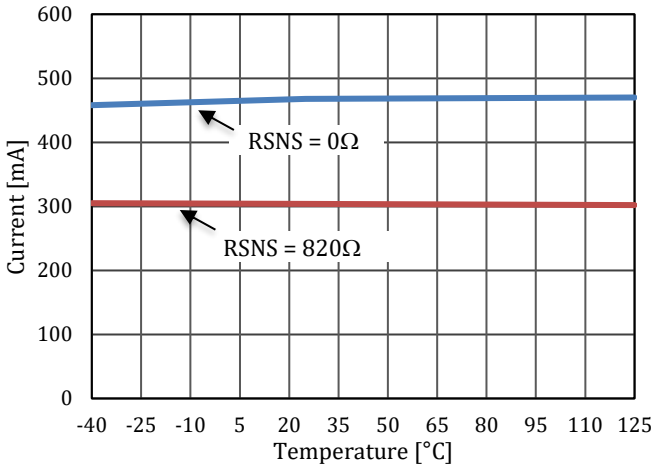


Figure 14 Current limit accuracy

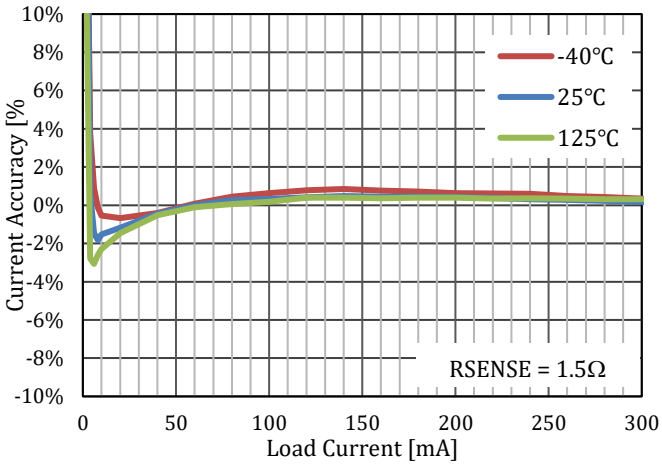


Figure 15 Current sense accuracy

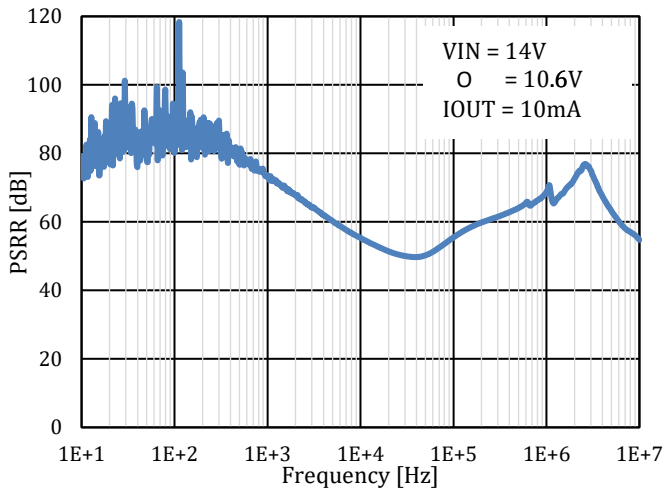


Figure 16 LDO1 PSRR

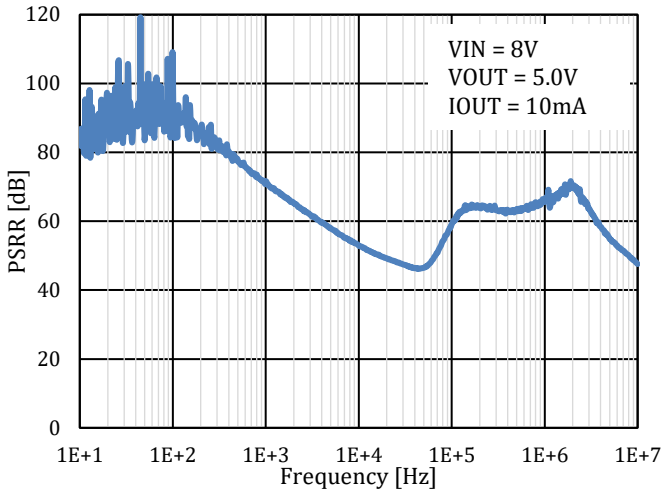


Figure 17 LDO2 PSRR

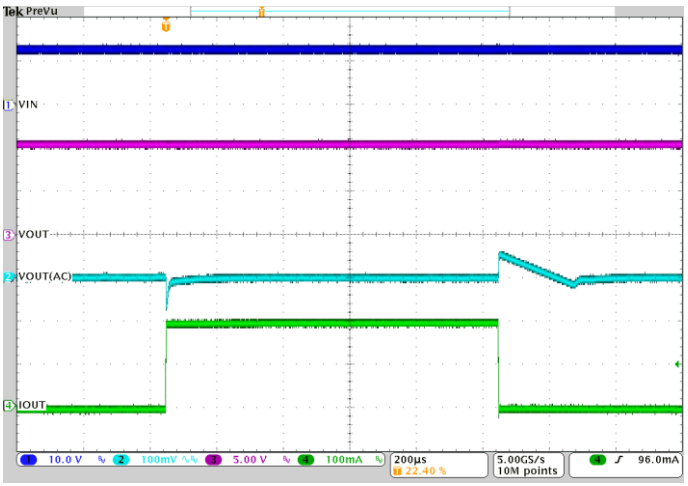


Figure 18 LDO1 Load transient

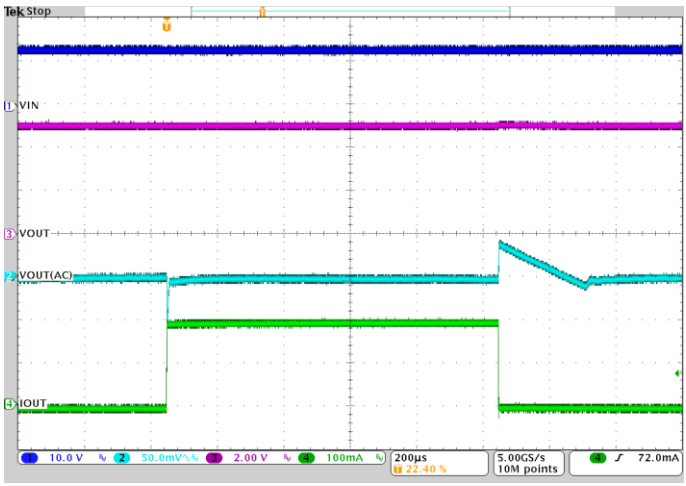


Figure 19 LDO2 Load transient

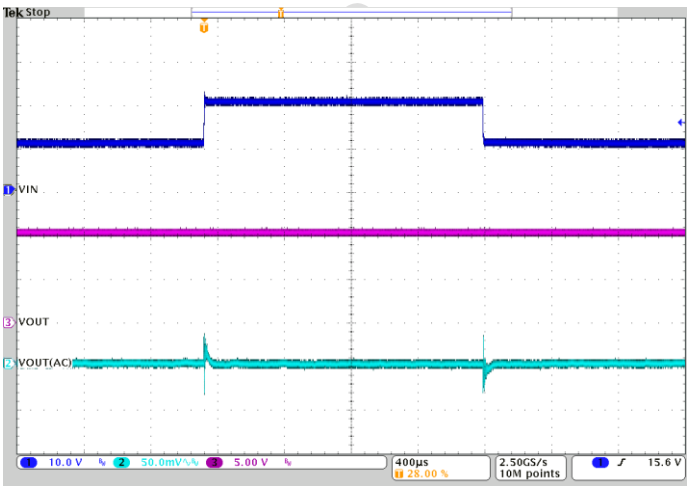


Figure 20 Line transient

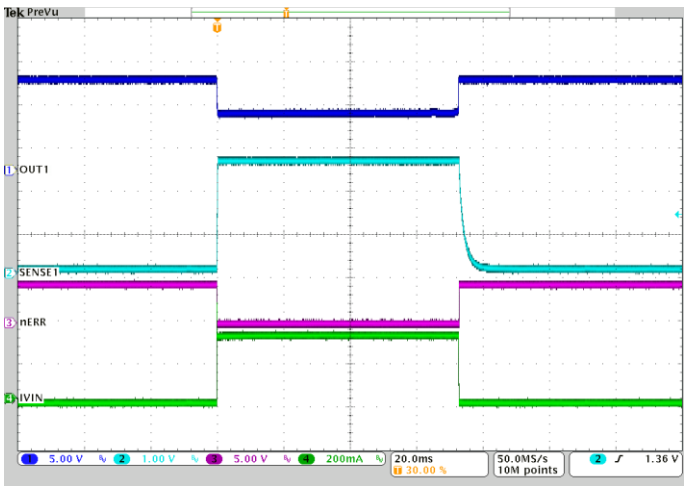


Figure 21 LDO Current limit

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