FAIRCHILD SEMICONDUCTOR®

February 2008

FSB52006S

Smart Power Module (SPM)

Features

- 60V, $R_{DS(ON).MAX}$=80mΩ @ 25°C 3-phase FRFET inverter including high voltage integrated circuit (HVIC)
- 3 divided negative dc-link terminals for inverter current sensing applications
- HVIC for gate driving and undervoltage protection
- 3/5V CMOS/TTL compatible, active-high interface
- Optimized for low electromagnetic interference
- Isolation voltage rating of 1500Vrms for 1min.
- Surface mounted device package
- Moisture Sensitive Level 3

General Description

FSB52006S is a tiny smart power module (SPM) based on FRFET technology as a compact inverter solution for small power motor drive applications such as fan motors and water suppliers. It is composed of 6 fast-recovery MOSFET (FRFET), and 3 half-bridge HVICs for FRFET gate driving. FSB52006S provides low electromagnetic interference (EMI) characteristics with optimized switching speed. Moreover, since it employs FRFET as a power switch, it has much better ruggedness and larger safe operation area (SOA) than that of an IGBT-based power module or one-chip solution. The package is optimized for the thermal performance and compactness for the use in the built-in motor application and any other application where the assembly space is concerned. FSB52006S is the most solution for the compact inverter providing the energy efficiency, compactness, and low electromagnetic interference.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Units
V_{PN}	DC Link Input Voltage, Drain-source Voltage of each FRFET		60	V
I_{D25}	Each FRFET Drain Current, Continuous	T_C = 25°C	2.6	A
I_{D100}	Each FRFET Drain Current, Continuous	T_C = 100°C	1.3	A
I_{DP}	Each FRFET Drain Current, Peak	T_C = 25°C, PW < 100μs	5	A
P_D	Maximum Power Dissipation	T_C = 25°C, Each FRFET	11	W
V_{CC}	Control Supply Voltage	Applied between V_{CC} and COM	20	V
V_{BS}	High-side Bias Voltage	Applied between $V_{B(U)}$-$V_{S(U)}$, $V_{B(V)}$-$V_{S(V)}$, $V_{B(W)}$-$V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between IN and COM	-0.3 ~ VCC+0.3	V
T_J	Operating Junction Temperature		-20 ~ 125	°C
T_{STG}	Storage Temperature		-50 ~ 150	°C
$R_{\theta JC}$	Junction to Case Thermal Resistance	Each FRFET under inverter operating condition (Note 1)	9.2	°C/W
V_{ISO}	Isolation Voltage	60Hz, Sinusoidal, 1 minute, Connection pins to heatsink	1500	V_{rms}

FAIRCHILD SEMICONDUCTOR®

February 2008

FSB52006S

Smart Power Module (SPM)

Features

- 60V, $R_{DS(ON).MAX}$=80mΩ @ 25°C 3-phase FRFET inverter including high voltage integrated circuit (HVIC)
- 3 divided negative dc-link terminals for inverter current sensing applications
- HVIC for gate driving and undervoltage protection
- 3/5V CMOS/TTL compatible, active-high interface
- Optimized for low electromagnetic interference
- Isolation voltage rating of 1500Vrms for 1min.
- Surface mounted device package
- Moisture Sensitive Level 3

General Description

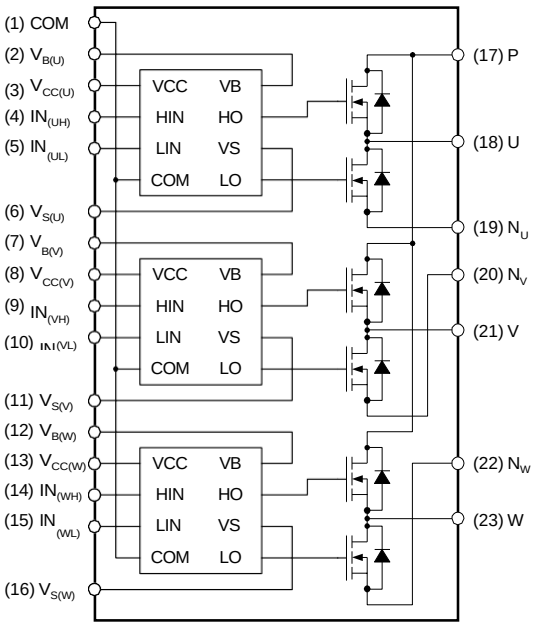
FSB52006S is a tiny smart power module (SPM) based on FRFET technology as a compact inverter solution for small power motor drive applications such as fan motors and water suppliers. It is composed of 6 fast-recovery MOSFET (FRFET), and 3 half-bridge HVICs for FRFET gate driving. FSB52006S provides low electromagnetic interference (EMI) characteristics with optimized switching speed. Moreover, since it employs FRFET as a power switch, it has much better ruggedness and larger safe operation area (SOA) than that of an IGBT-based power module or one-chip solution. The package is optimized for the thermal performance and compactness for the use in the built-in motor application and any other application where the assembly space is concerned. FSB52006S is the most solution for the compact inverter providing the energy efficiency, compactness, and low electromagnetic interference.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Units
V_{PN}	DC Link Input Voltage, Drain-source Voltage of each FRFET		60	V
I_{D25}	Each FRFET Drain Current, Continuous	T_C = 25°C	2.6	A
I_{D100}	Each FRFET Drain Current, Continuous	T_C = 100°C	1.3	A
I_{DP}	Each FRFET Drain Current, Peak	T_C = 25°C, PW < 100μs	5	A
P_D	Maximum Power Dissipation	T_C = 25°C, Each FRFET	11	W
V_{CC}	Control Supply Voltage	Applied between V_{CC} and COM	20	V
V_{BS}	High-side Bias Voltage	Applied between $V_{B(U)}$-$V_{S(U)}$, $V_{B(V)}$-$V_{S(V)}$, $V_{B(W)}$-$V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between IN and COM	-0.3 ~ VCC+0.3	V
T_J	Operating Junction Temperature		-20 ~ 125	°C
T_{STG}	Storage Temperature		-50 ~ 150	°C
$R_{\theta JC}$	Junction to Case Thermal Resistance	Each FRFET under inverter operating condition (Note 1)	9.2	°C/W
V_{ISO}	Isolation Voltage	60Hz, Sinusoidal, 1 minute, Connection pins to heatsink	1500	V_{rms}

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	$V_{B(U)}$	Bias Voltage for U Phase High Side FRFET Driving
3	$V_{CC(U)}$	Bias Voltage for U Phase IC and Low Side FRFET Driving
4	$IN_{(UH)}$	Signal Input for U Phase High-side
5	$IN_{(UL)}$	Signal Input for U Phase Low-side
6	$V_{S(U)}$	Bias Voltage Ground for U Phase High Side FRFET Driving
7	$V_{B(V)}$	Bias Voltage for V Phase High Side FRFET Driving
8	$V_{CC(V)}$	Bias Voltage for V Phase IC and Low Side FRFET Driving
9	$IN_{(VH)}$	Signal Input for V Phase High-side
10	$IN_{(VL)}$	Signal Input for V Phase Low-side
11	$V_{S(V)}$	Bias Voltage Ground for V Phase High Side FRFET Driving
12	$V_{B(W)}$	Bias Voltage for W Phase High Side FRFET Driving
13	$V_{CC(W)}$	Bias Voltage for W Phase IC and Low Side FRFET Driving
14	$IN_{(WH)}$	Signal Input for W Phase High-side
15	$IN_{(WL)}$	Signal Input for W Phase Low-side
16	$V_{S(W)}$	Bias Voltage Ground for W Phase High Side FRFET Driving
17	P	Positive DC–Link Input
18	U, $V_{S(U)}$	Output for U Phase & Bias Voltage Ground for High Side FRFET Driving
19	N_U	Negative DC–Link Input for U Phase
20	N_V	Negative DC–Link Input for V Phase
21	V, $V_{S(V)}$	Output for V Phase & Bias Voltage Ground for High Side FRFET Driving
22	N_W	Negative DC–Link Input for W Phase
23	W, $V_{S(W)}$	Output for W Phase & Bias Voltage Ground for High Side FRFET Driving

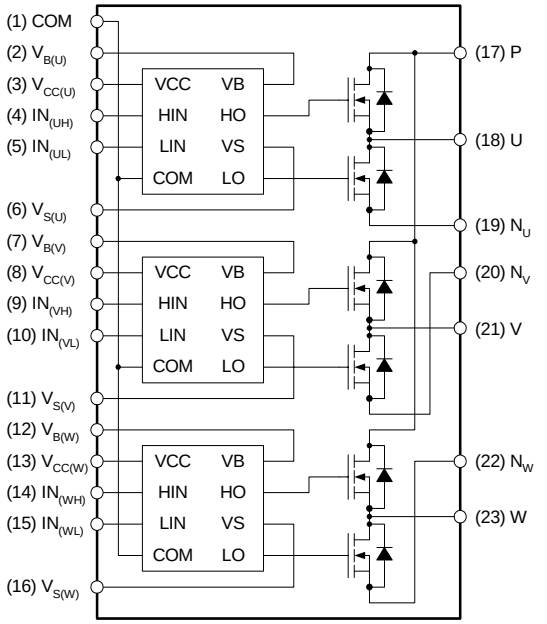


Note:
Source terminal of each MOSFET is not connected to supply ground or bias voltage ground inside SPM. External connections should be made as indicated in Figure 2 and 5.

Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	$V_{B(U)}$	Bias Voltage for U Phase High Side FRFET Driving
3	$V_{CC(U)}$	Bias Voltage for U Phase IC and Low Side FRFET Driving
4	$IN_{(UH)}$	Signal Input for U Phase High-side
5	$IN_{(UL)}$	Signal Input for U Phase Low-side
6	$V_{S(U)}$	Bias Voltage Ground for U Phase High Side FRFET Driving
7	$V_{B(V)}$	Bias Voltage for V Phase High Side FRFET Driving
8	$V_{CC(V)}$	Bias Voltage for V Phase IC and Low Side FRFET Driving
9	$IN_{(VH)}$	Signal Input for V Phase High-side
10	$IN_{(VL)}$	Signal Input for V Phase Low-side
11	$V_{S(V)}$	Bias Voltage Ground for V Phase High Side FRFET Driving
12	$V_{B(W)}$	Bias Voltage for W Phase High Side FRFET Driving
13	$V_{CC(W)}$	Bias Voltage for W Phase IC and Low Side FRFET Driving
14	$IN_{(WH)}$	Signal Input for W Phase High-side
15	$IN_{(WL)}$	Signal Input for W Phase Low-side
16	$V_{S(W)}$	Bias Voltage Ground for W Phase High Side FRFET Driving
17	P	Positive DC–Link Input
18	U, $V_{S(U)}$	Output for U Phase & Bias Voltage Ground for High Side FRFET Driving
19	N_U	Negative DC–Link Input for U Phase
20	N_V	Negative DC–Link Input for V Phase
21	V, $V_{S(V)}$	Output for V Phase & Bias Voltage Ground for High Side FRFET Driving
22	N_W	Negative DC–Link Input for W Phase
23	W, $V_{S(W)}$	Output for W Phase & Bias Voltage Ground for High Side FRFET Driving



Note:
Source terminal of each MOSFET is not connected to supply ground or bias voltage ground inside SPM. External connections should be made as indicated in Figure 2 and 5.

Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)