PC8818
Single Channel 80mΩ High Side Switch

1 Overview

PC8818 is a 80mΩ $R_{DS\ (ON)}$ high side switch, providing fully protections and diagnostic functions. This device has two versions. For version A, the device reports the fault condition with the FLTn pin, open-drain structure.

For version B, its ISNS pin outputs a small current proportional to the current flowing through the internal power FET. The user can connect a resistor from ISNS pin to GND. Then monitoring the voltage of this resistor, the user will know the load conditions, such as normal operation, short to ground, open load, etc..

The device limits the current flowing through its internal power FET. The current limit level can be set with an external resistor from the ILIM pin to the ground. An internal charge pump drives the gate of the power FET, allowing a typical 80 mΩ $R_{DS\ (ON)}$. When the output current is over the current limit setting, the device regulates the power FET to clamp the output current at the setting level. When connecting the ILIM pin to the ground, the current limit is the internal default value. The active of the current limit circuit causes the power consumption of the device increases. The thermal accumulation of the device may trigger the thermal shutdown, turning off the power FET. When the power FET is turned off, the power path is disconnected, then the device temperature will decrease. When the device cools down, it will turn on the power FET again.

PC8818 is available in a HTSSOP-14L package with exposed thermal pad.

2 Overview

- Operating voltage range, 3.5V ~ 40 V
- Very-low standby current, <0.5 μA
- AEC-Q100 Qualified:
  - Device temperature grade 1: –40°C to 125°C
- Operating junction temperature, –40°C to 150°C
- 3.3 V and 5V compatible control logic
- High-accuracy current sense, ±30 mA at 1 A
- Programmable current limit with external resistor
- Diagnostic function can be enabled or disabled
- Tested according to AECQ100-12 Grade A, 1 million times Short to GND test
- Electrical transient disturbance immunity certification of ISO7637-2 and ISO16750-2
- Protections
  - Overload and short-circuit protection
  - Inductive load negative voltage clamp
  - Undervoltage lockout (UVLO) protection
  - Thermal shutdown/swing with self-recovery
  - Loss of GND, loss of supply protection
  - Reverse battery protection with external circuitry
- Diagnosis
  - On- and Off-state output open and short to battery detection
  - Overload and short to ground detection and current limit
  - Thermal shutdown/swing detection
- Diagnosis reports
  - Version A: open-drain digital output
  - Version B: current sense analog output
- HTSSOP-14L

3 Applications

- Power switch for low wattage lamp
- High side relays and valve
- General resistive, inductive, and capacitive loads

4 Typical Application Diagram

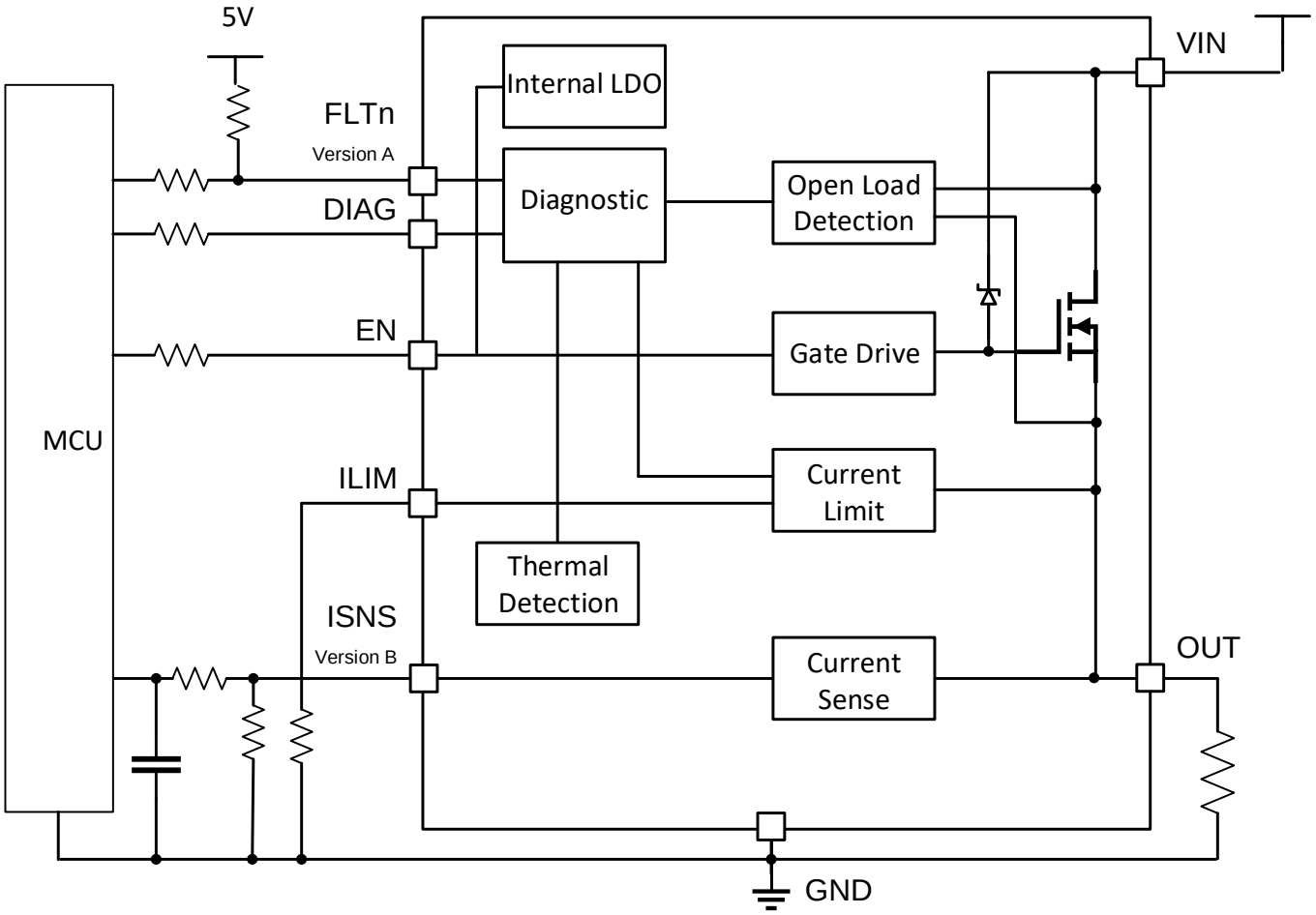

Figure 4-1. Typical System Diagram

5 Ordering Information

Table 5-1: Ordering Part Number

PART NUMBER	No. of Channel	Ron	Diagnose	Package
PC8818SCAQ1	1	80mΩ	Digital IO (FLTn)	HTSSOP-14
PC8818SCBQ1	1	80mΩ	Analog Output (ISNS)	HTSSOP-14

6 Functional Block Diagram

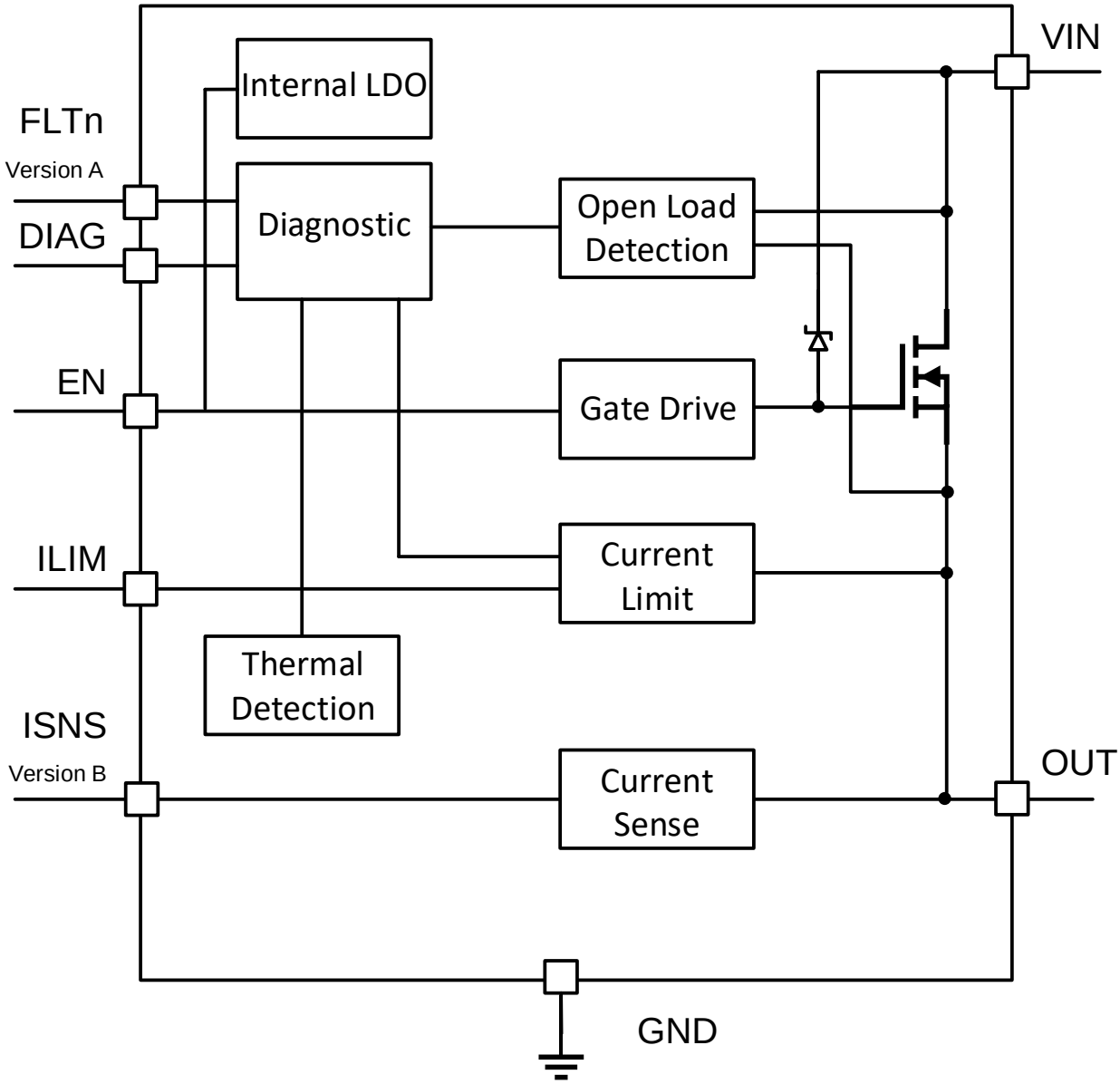

Figure 6-1. Functional Block Diagram

7 Pin Diagram

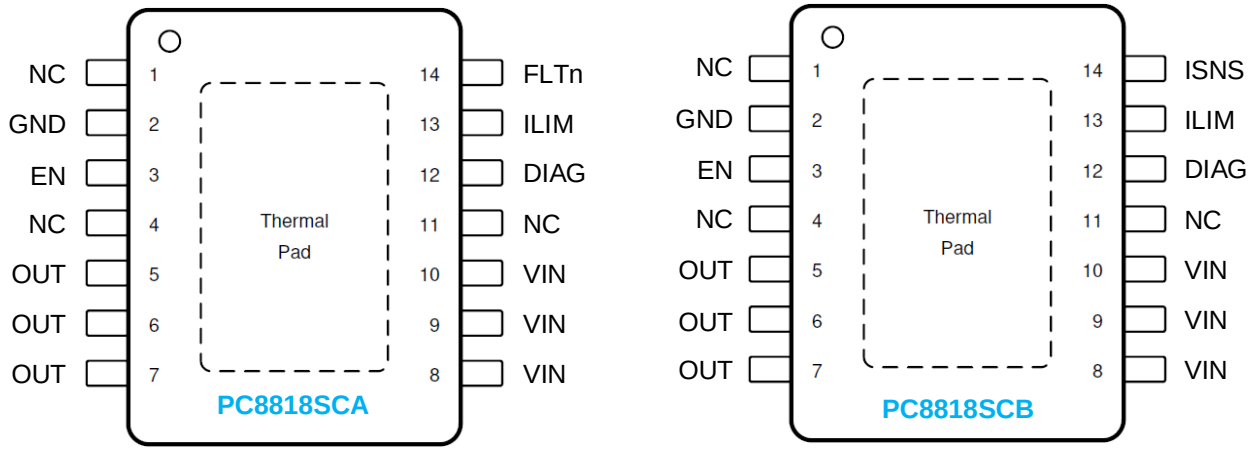

Figure 7-1. PC8818 Pin Map

7.1 Pin Description

Table 7-1 Pin description

Pin Name	Pin Type	Product Version		Description
		Version A	Version B	
ILIM	Output	13	13	Current limit pin. Program the current limit level by connecting a resistor from this pin to the ground. If directly connects the pin to the ground, using the internal current limit level.
ISNS	Output	—	14	Current sense pin. Output a current proportional to the output current. Leave floating if not used.
DIAG	Input	12	12	Enable and disable pin for diagnostic functions. Connect to device GND if not used.
GND	—	2	2	Ground pin
EN	Input	3	3	Enable and disable pin for power FET control.
NC	—	1,4,11	1,4,11	No-connect pin; leave floating.
OUT	Output	5,6,7	5,6,7	Output pin, connected to load.
FLTn	Output	14	—	Diagnosis digital output pin, Open-drain structure. Leave floating if not used.
VIN	Power Supply	8,9,10	8,9,10	Power supply
Thermal Pad	—	—	—	Thermal pad. Connect to device GND or leave floating.

7.2 Pin Voltage and Current Definition

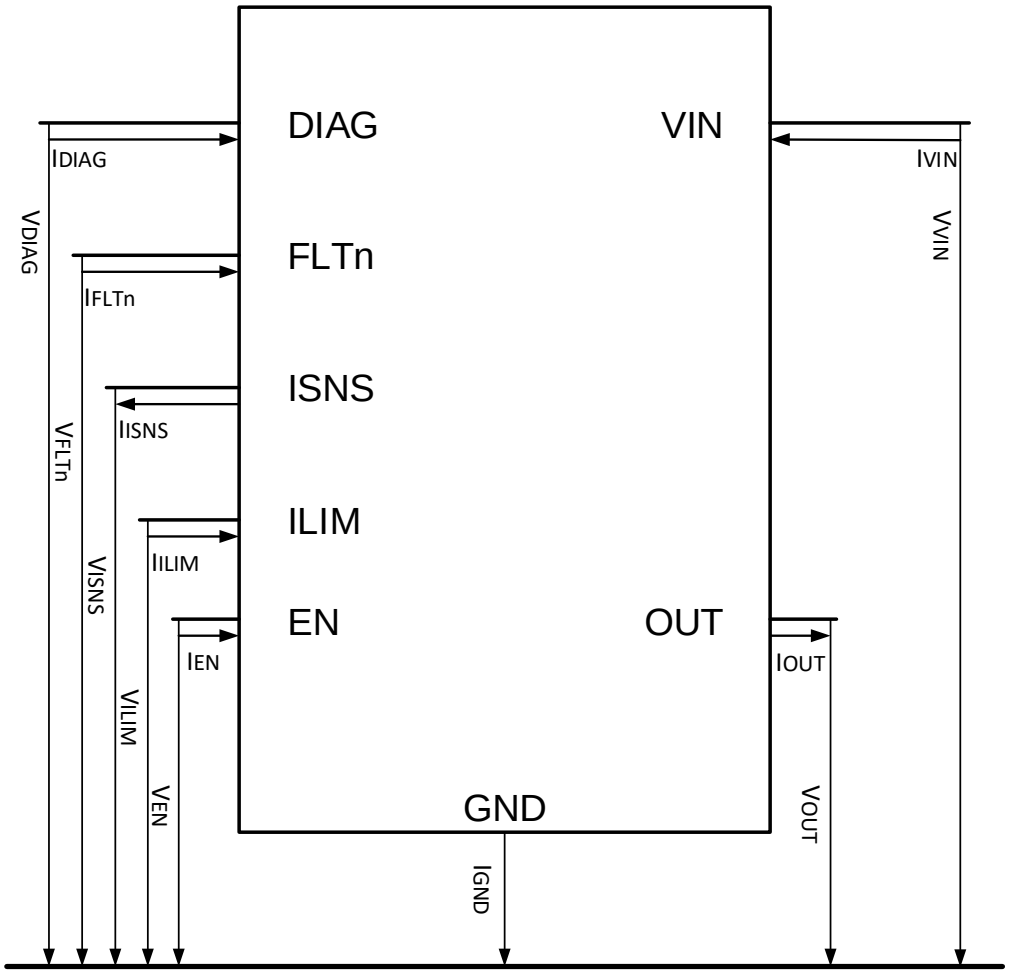

Figure 7-2. Pin Voltage and Current Definition

8 Specifications

8.1 Absolute Maximum Ratings (1)(2)

Parameters		MIN	MAX	Unit
Voltage range	VIN pin	-18(3)	42	V
	EN, DIAG, FLTn, ILIM and ISNS pins	-1	7	V
Pin current	GND pin	-50	20	mA
	GND pin, t<120 s	-250	20	mA
	EN and DIAG pins	-30	2	mA
	FLTn pin	-30	10	mA
	ILIM and ISNS pins	-2	30	mA
EN pin switching frequency			2	KHz
Inductive load switch-off energy dissipation, single pulse (4)			70	mJ
Operating ambient temperature, T_A		-40	125	°C
Operating junction temperature, T_J		-40	150	°C
Storage temperature, T_{STG}		-65	150	°C
ESD	HBM, AEC-Q100 Level H3A (5), VIN, OUT and GND pins.	±5000		V
	HBM, AEC-Q100 Level H2A (5), other pins	±4000		V
	CDM, AEC-Q100-011 (6)	±750		V

8.2 Recommended Operating Conditions (2)(7)

Parameters		MIN	MAX	Unit
Pin Voltage	VIN, Operating Voltage	5	40	V
	EN, DIAG, FLTn	0	5	V
Continuous output current		0	4	A
Operating junction temperature, T_J		-40	150	°C

NOTE:

1. Stress beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. All voltage values are with respect to network ground.
3. Reverse polarity condition: t < 60 s, reverse current < Irev1, GND pin 1kΩ resistor in parallel with diode.
4. Test condition: VIN = 13.5 V, L = 8 mH, R = 0 Ω, T_J = 150°C. FR4 2s2p board, 2 × 70μm Cu, 2 × 35μm Cu. 600 mm2 thermal pad copper area.
5. The human-body model is a 107pF capacitor discharged through a 1.5kΩ resistor into each terminal.
6. The charged-device model is tested according to AEC Q100-011C.
7. Functional operation of the device at any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.3 Thermal Information

Thermal Resistance	Package HTSSOP-14	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	47.8	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	27.3	°C/W
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	4.9	°C/W

The thermal data is based on JEDEC standard high-K profile – JESD 51-7. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.

NOTE:

(1) 4 layers board: FR4 2s2p board, 2.8-mil copper (top/bottom), 1.4mil copper (internal layers). 76.4× 114.3× 1.5mm board size.
(2) 2 layers board: FR4 2s0p board, 2.8-mil copper (top/bottom). 76.4 × 114.3 × 1.5mm board size.

8.4 Electrical Specification

5 V < V_{VIN} < 40 V; –40°C < T_J < 150°C unless otherwise specified.

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	UNIT
VIN (INPUT SUPPLY)						
VIN	operating voltage		5		40	V
$VIN_{\_EXT}$	Extended operating voltage	compared to 5 V, $R_{DS(on)}$ value increases maximum 20%	3.5		5	V
V_{UVR}	Undervoltage rising threshold	V_{VIN}> V_{UVR}, device turn on	3.5	3.85	4	V
V_{UVF}	Undervoltage falling threshold	V_{VIN}< V_{UVF}, device shuts off	3.0	3.19	3.5	V
$V_{UV,hys}$	Undervoltage hysteresis			0.65		V
I_{nom}	Operation current	V_{EN} = 5 V, V_{DIAG} = 0 V, V_{VIN}=13.5 V			5	mA
		V_{EN} = 5 V, V_{DIAG} = 0 V, V_{VIN}=13.5 V, 0.1A load, ground current			10	mA
I_{OFF}	Standby current	V_{VIN} = 13.5 V, V_{EN} = V_{DIAG} = V_{ISNS} = V_{ILIM} =V_{OUTPUT} = 0 V, T_J = 25°C			0.5	uA
		V_{VIN} = 13.5 V, V_{EN} = V_{DIAG} = V_{ISNS} = V_{ILIM} =V_{OUTPUT} = 0 V, T_J = 125°C			5	uA
I_{OFF_diag}	Standby current with diagnostic enabled	V_{EN} = 0 V, V_{DIAG} = 5 V, V_{VIN}=13.5V, no load			1.2	mA
t_{OFF_deg}	Standby mode deglitch time (1)	EN from high to low, if deglitch time > t_{OFF_deg}, enters into standby mode.		2		ms
I_{OUT_lkg}	Off-state output leakage current	V_{VIN} = 13.5 V, V_{EN} = V_{OUTPUT} = 0 V, T_J = 25°C			0.3	uA
		V_{VIN} = 13.5 V, V_{EN} = V_{OUTPUT} = 0 V, T_J = 125°C			3	uA
Power Stage						
$R_{DS(ON)}$	On-state resistance	V_{VIN} > 5 V, T_J = 25°C		80	100	mΩ
		V_{VIN} > 5 V, T_J = 150°C			166	mΩ
		V_{VIN} = 3.5 V, T_J = 25°C			120	mΩ
I_{LIM_int}	Internal current limit		7		13	A
V_{DS_cl}	drain to source clamp voltage		43		50	V
V_F	Drain to source diode voltage	V_{EN} = 0, I_{OUT} = −0.2 A		0.6		V
I_{rev1}	Continuous reverse current when reverse polarity (2)	t < 60 s, V_{VIN} = 13.5 V, GND pin network 1kΩ resistor in parallel with diode. T_J = 25°C. See I_{rev1} test condition (Figure 8-2)		4		A
I_{rev2}	Continuous reverse current when V_{OUT} > V_{VIN} + V_{diode} (2)	t < 60 s, V_{VIN} = 13.5 V. T_J = 25°C. See I_{rev2} test condition (Figure 8-3).		2		A
LOGIC INPUT (EN AND DIAG)						
V_{logic_h}	EN or DIAG high-level voltage		2			V
V_{logic_l},	EN or DIAG low-level voltage				0.8	V
V_{logic_hys}	EN or DIAG hysteresis voltage			150		mV
R_{pd_EN},	EN pin pulldown resistor			360		kΩ
R_{pd_DIAG},	DIAG pin pulldown resistor			110		kΩ
DIAGNOSTICS						
I_{loss_GND}	Loss of ground output leakage current				100	uA
V_{OL_Off}	Open load detection threshold in off-state	V_{EN} = 0 V, If V_{VIN} – V_{OUT} < V_{OL_Off}, duration longer than t_{OL_Off}. Open load detected.	1.4	2.2	2.7	V
I_{OL_Off}	Open load Off-state output sink current	V_{EN} = 0 V, V_{VIN} = V_{OUT} = 13.5 V, T_J = 125°C.			-50	uA
V_{FLTn}	Output low voltage	I_{FLTn} = 2 mA. Version A only			0.4	V
t_{OL_Off}	Open load detection threshold deglitch time in off-state	V_{EN} = 0 V, If V_{VIN} – V_{OUT} < V_{OL_Off}, duration longer than t_{OL_Off}. Open load detected.		600		us
I_{OL_On}	Open load detection in on state	V_{EN} = 5 V, if I_{OUT} < I_{OL_On}, duration longer than t_{OL_On}. Open load detected. Version A only	2	6	10	mA

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	UNIT
t_{OL_On}	Open load detection threshold deglitch time in on state	V_{EN} = 5 V, if I_{OUT} < I_{OL_On}, duration longer than t_{OL_On}. Open load detected. Version A only		700		us
T_{SD}	Thermal shutdown threshold			175		°C
T_{SD_rst},	Thermal shutdown status reset			145		
T_{sw}	Thermal swing shutdown threshold			60		
T_{hys}	Hysteresis for resetting the thermal swing			10		
CURRENT SENSE (VERSION B) AND CURRENT LIMIT						
K	Current sense current ratio			500		
K_{ILIM}	Current limit current ratio			4000		
dK/K	Current sense accuracy	I_{load} ≥ 5 mA	-80		80	%
		I_{load} ≥ 25 mA	-10		10	
		I_{load} ≥ 50 mA	-7		7	
		I_{load} ≥ 0.1A	-5		5	
		I_{load} ≥ 1A	-3		3	
dK_{ILIM}/K_{ILIM}	External current limit accuracy (3	I_{lim} ≥ 0.5A	-20		20	%
		I_{lim} ≥ 1.6A	-14		14	
V_{ISNS_lin}	Linear current sense voltage range (1)	V_{VIN} ≥ 5 V	0		4	V
$I_{OUT,lin}$	Linear output current range (1)	V_{VIN} ≥ 5 V, V_{ISNS_lin} ≤ 4 V	0		4	A
V_{ISNS_H}	Current sense fault high voltage	V_{VIN} ≥ 7 V	4.3	4.75	4.9	V
		V_{VIN} ≥ 5 V	Min (V_{VIN} – 0.8, 4.3)		4.9	V
I_{ISNS_H}	Current sense fault condition current	V_{ISNS} = 4.3 V, V_{VIN} > 7 V	10			mA
V_{ILIM_th}	Current limit internal threshold voltage (1)			0.616		V
I_{ISNS_LKG}	Current sense leakage current in disabled mode	V_{EN} = 0 V, V_{DIAG} = 0 V, T_J = 125°C			1	uA

NOTE:

1. These parameters are guaranteed by design and are not subject to production test.
2. Value is based on the minimum value of the 10 pcs/3 lots samples.
3. External current-limit setting is recommended to be higher than 500 mA.

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	UNIT
Timing Requirements (1)						
t_{ISNS_off1}	ISNS settling time from DIAG disabled	V_{EN} = 5 V, I_{load} ≥ 5 mA. V_{DIAG} from 5V to 0 V. ISNS to 10% of sense value. (Figure 8-4).			10	us
t_{ISNS_on1}	ISNS settling time from DIAG enabled	V_{EN} = 5 V, I_{load} ≥ 5 mA. V_{DIAG} from 0V to 5 V. ISNS to 90% of sense value. (Figure 8-4).			85	us
t_{ISNS_off2}	ISNS settling time from EN falling edge	V_{DIAG} = 5 V, I_{load} ≥ 5 mA. V_{EN} from 5V to 0 V. ISNS to 10% of sense value. (Figure 8-4).			45	us
		V_{DIAG} = 5 V, I_{load} ≥ 5 mA. V_{EN} from 5V to 0 V. Current limit triggered. (Figure 8-4).			180	us
t_{ISNS_on2}	ISNS settling time from EN rising edge	V_{VIN} = 13.5 V, V_{DIAG} = 5 V, I_{load} ≥ 100 mA. V_{EN} from 0 to 5 V. ISNS to 90% of sense value. (Figure 8-4).			150	us
t_{d_ON}	Turn-on delay time	EN rising edge to V_{OUT} = 10%, V_{DIAG} high. (Figure 8-6).	20		50	us
t_{d_OFF}	Turn-off delay time	EN falling edge to V_{OUT} = 90%, V_{DIAG} high. (Figure 8-6).	20		50	us
$dV/dt_{ON,}$	Slew rate on	V_{OUT} = 10% to 90%, V_{DIAG} high. (Figure 8-6).	0.1		0.5	V/µs
dV/dt_{OFF}	Slew rate off	V_{OUT} = 90% to 10%, V_{DIAG} high. (Figure 8-6).	0.1		0.5	V/µs
	Slew rate on and off matching		-0.15		0.15	V/µs

NOTE:

1. These parameters are guaranteed by design and are not subject to production test.

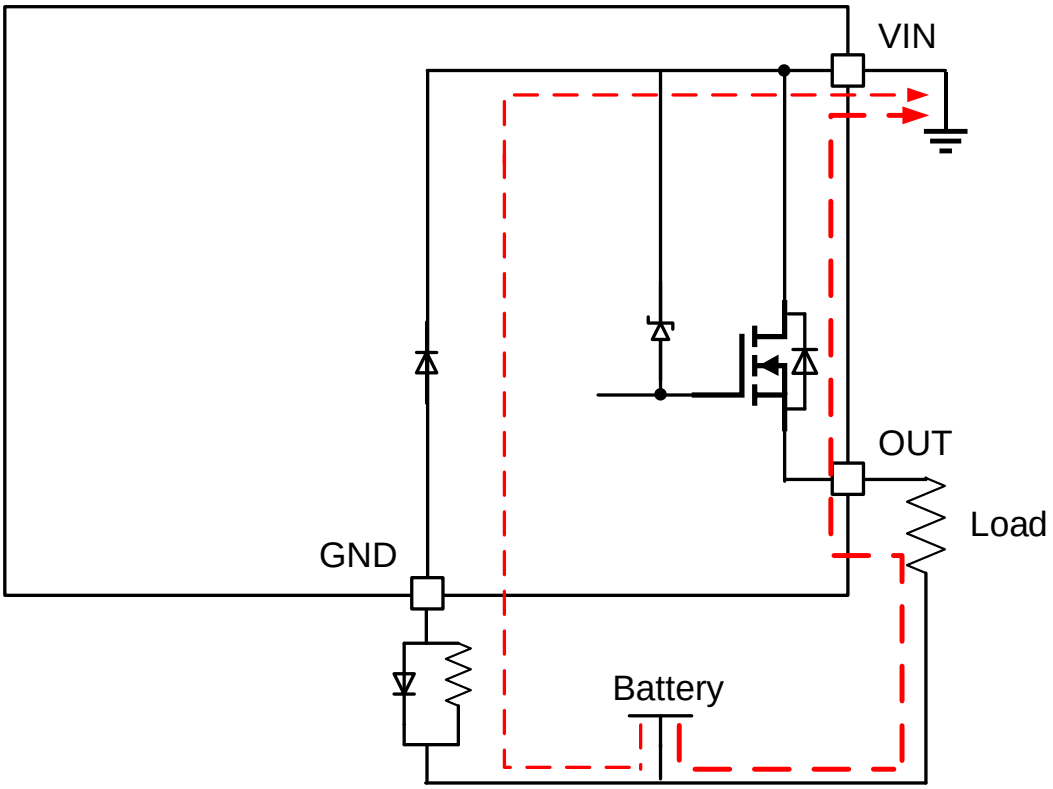

Figure 8-2. Irev1 Test Condition

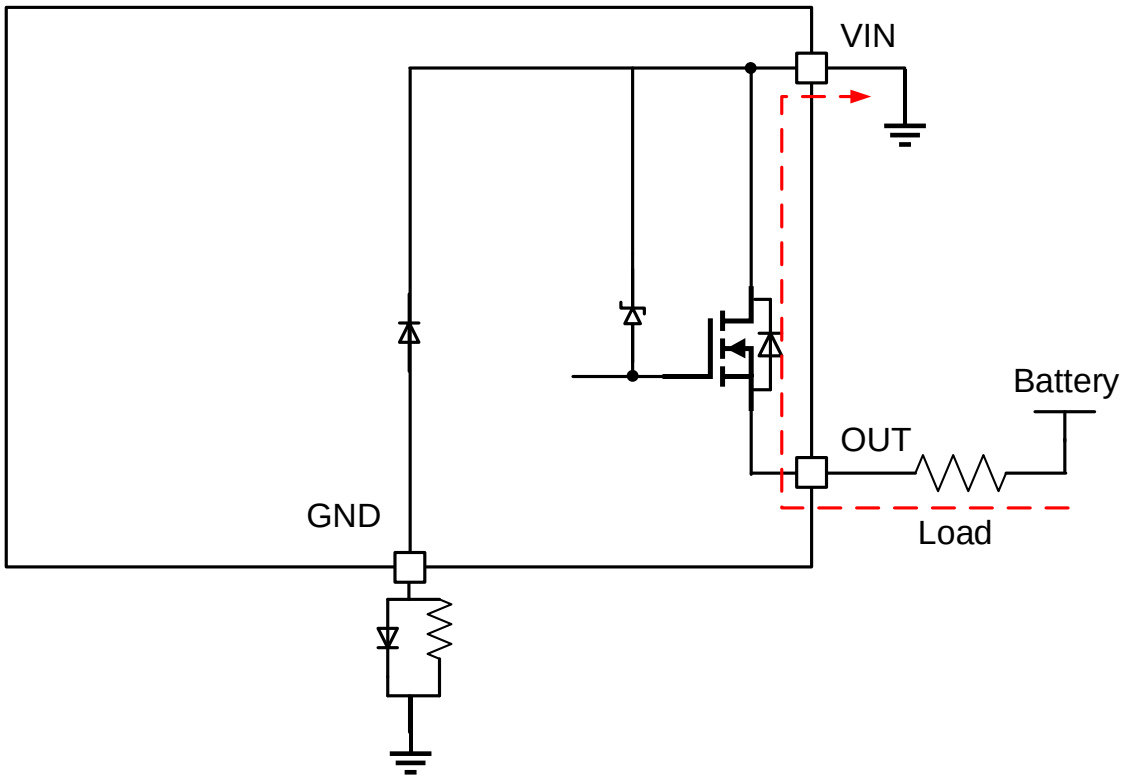

Figure 8-3. Irev2 test condition

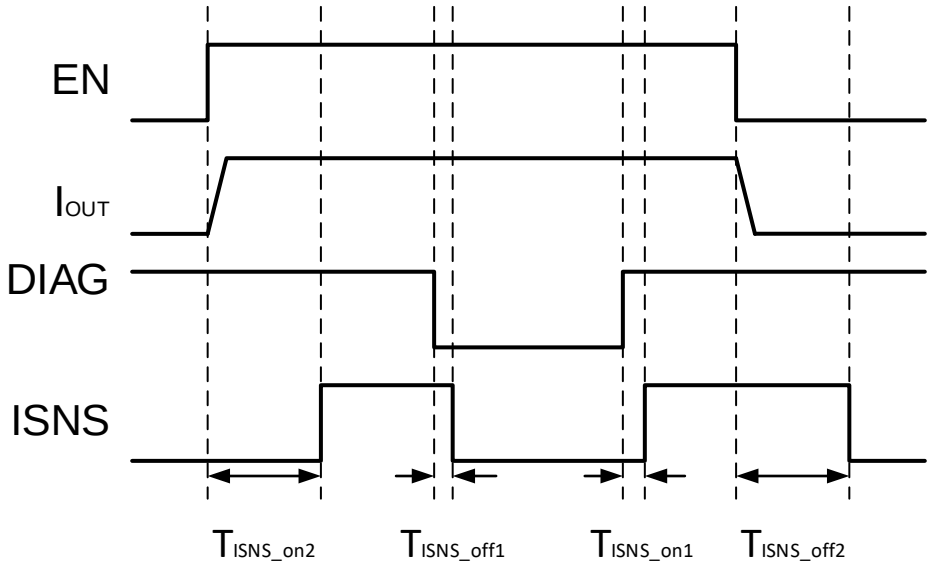

Figure 8-4. ISNS Delay Characteristics

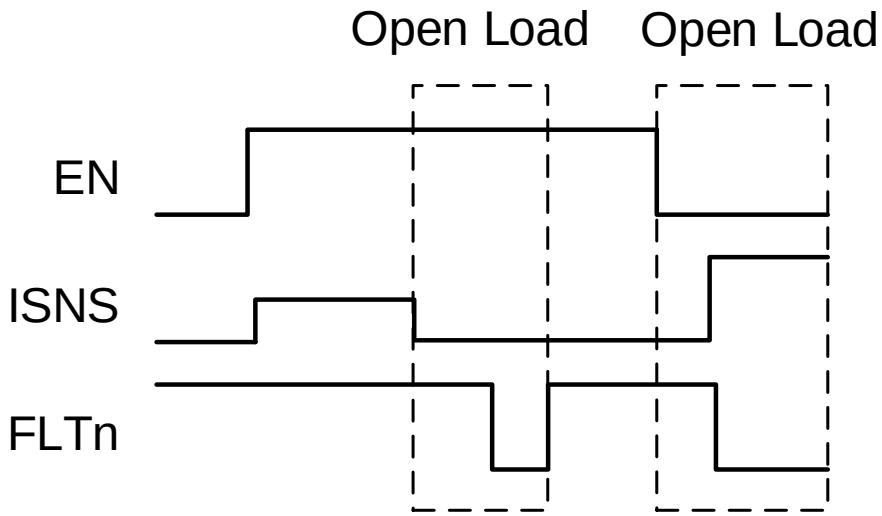

Figure 8-5. Open Load Blanking Time Characteristics

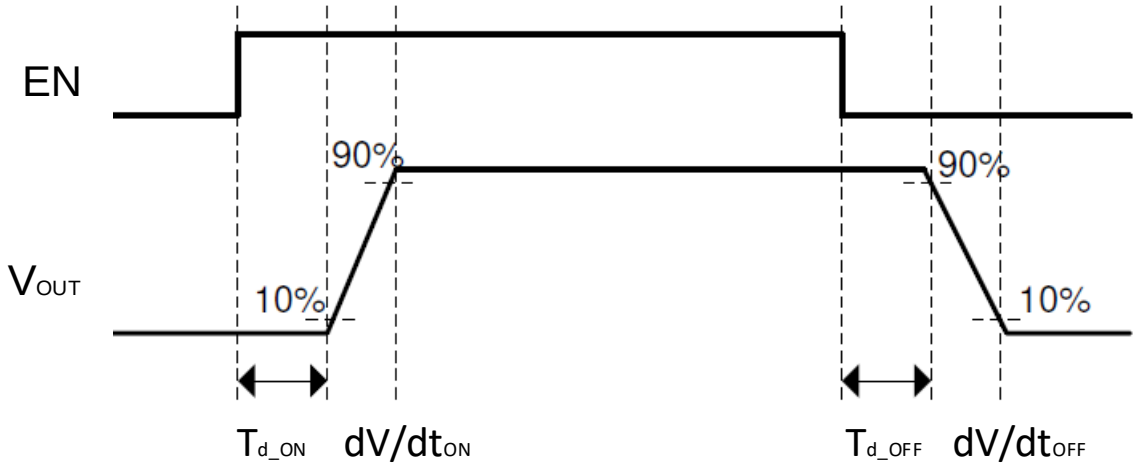

Figure 8-6. Switching Characteristics

9 Typical Operating Characteristics

10 Detailed Description

10.1 Overview

The PC8818 is a single channel, high side power switch with typical 80mΩ $R_{DS(ON)}$ power FETs. The device offers diagnosis, full protections and high precision current detection function, it can realize intelligent control of the load and improve the safety level of the system. There are two versions of the device. For Version A, the device output the digital diagnosis from the FLTn pin, an open drain structure. When a fault condition occurs, it pulls down to GND. An external pullup resistor connecting to 3.3V or 5V power rail is required to match the microcontroller I/O voltage level. For Version B, the device outputs a current from the ISNS pin which is 1/K ratio of the load current. The ISNS pin can also report a fault by pulling up the voltage of V_{ISNS_h}. When the DIAG pins is pulled low, the FLTn/ISNS pin is set to a high impedance state.

Connecting an external resistor from ILIM pin to GND allows setting the accurate current limit. Through precise control of the current, the inrush current during the startup process or the short-circuit current during the output hard short is limited, which greatly improves the reliability of the system. And reduce the design redundancy required to deal with these abnormal conditions, thereby saving the system cost. The device also implements an internal current limit. The lower value of the external or internal current-limit value is applied.

An internal power FET drain to source voltage clamp is implemented to address the switching off energy of the inductive loads, such as relays, valve, motors, etc.. During the inductive load switching off cycle, both the energy of the power supply (E_{BAT}) and the load (E_{LOAD}) are dissipated on the high side power switch itself. The PC8818 can achieve excellent power dissipation capacity, which can help save the external free-wheeling circuitry in most cases. See *Switching off the Inductive Load* for more details.

In automotive application scenarios, the short-circuit reliability of the high side power switch device is critical. To this end, the AEC Q100-012 defines the test standard for the device continuous short. Different levels are divided according to the number of the pass cycles. The device is certified to the highest level, Class A, 1 million shorts to ground.

The PC8818 device can be used as a high side power switch for a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, relays, and valves, etc..

10.2 Accurate Current Sensing

For version B, the device outputs an accurate current proportional to the load current, which allows a real time output status monitor and more accurate diagnostics. A current mirror circuit is used to source 1 / K of the load current, flowing out to the external resistor between the ISNS pin and GND.

K is the ratio of the output current and the ISNS pin current. It is a constant value across the temperature and supply voltage.

Ensure the ISNS voltage is in the linear region (0 to 4 V) during normal operation. Calculate R_{ISNS} with Equation 1.

$$R_{ISNS} = \frac{V_{ISNS}}{I_{ISNS}} = \frac{V_{ISNS} \times K}{I_{OUT}} \quad (1)$$

When a fault condition occurs, ISNS also works as a diagnostics report pin. When an open load or short to battery occurs in the on-state, V_{ISNS} almost equals 0. When current limit, thermal shutdown/swing, open load, or short to battery occurs in the off-state, the voltage is pulled up to V_{ISNS_h}. Figure 10-2 shows a typical current-sense voltage according to the operating conditions, including fault conditions.

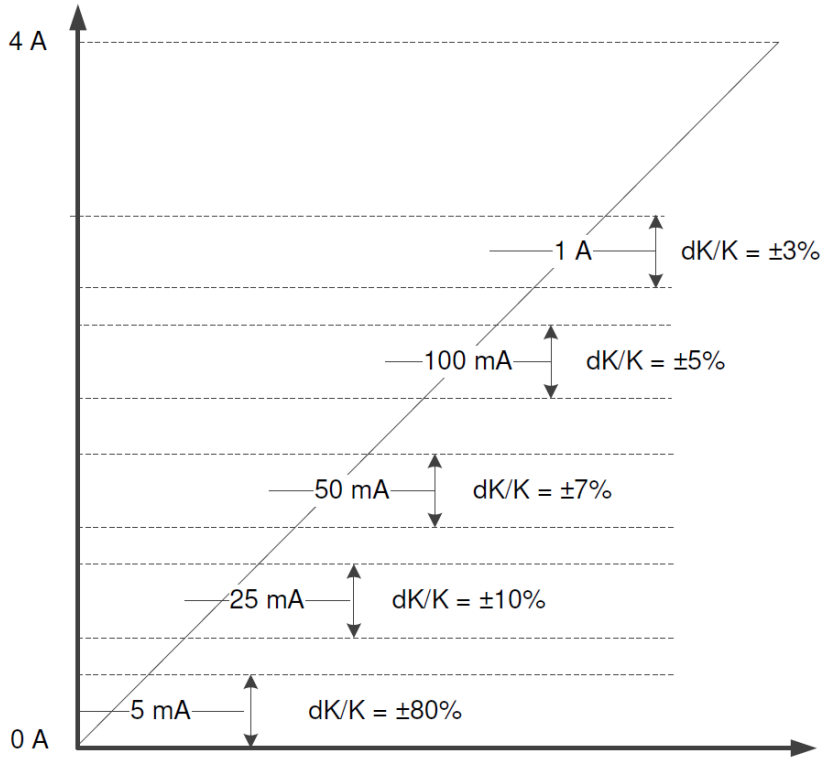

Figure 10-1 Current Sense Accuracy

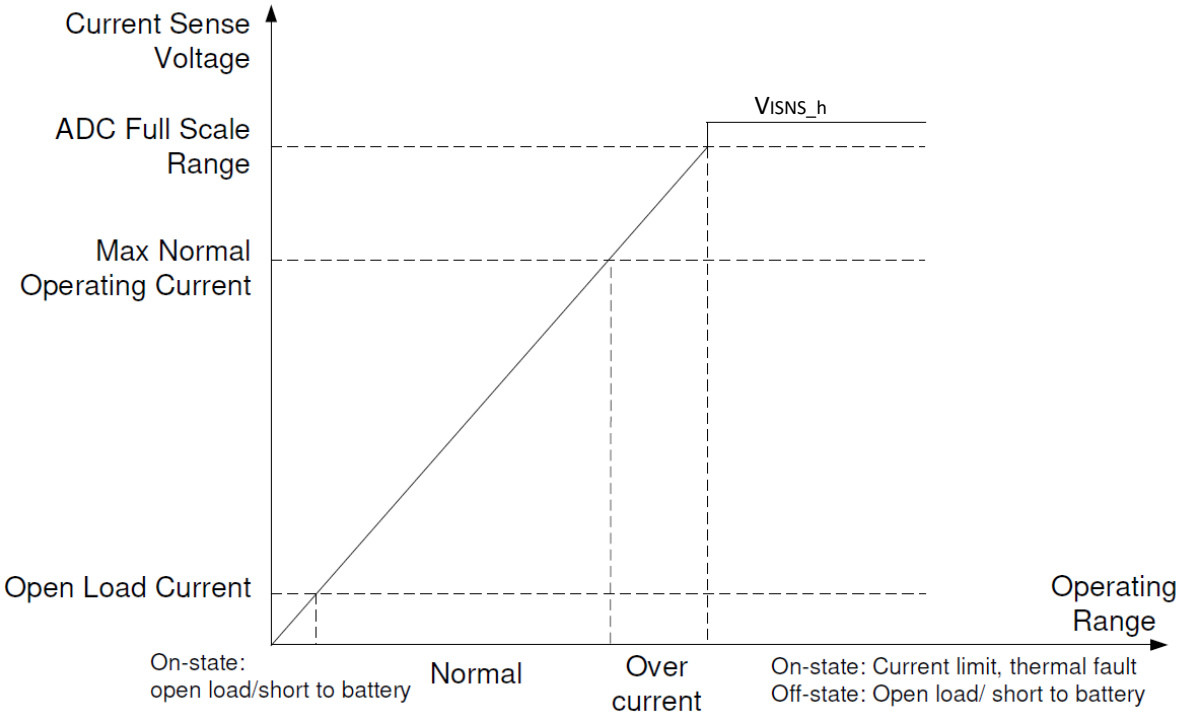

Figure 10-2. Voltage on the ISNS pin

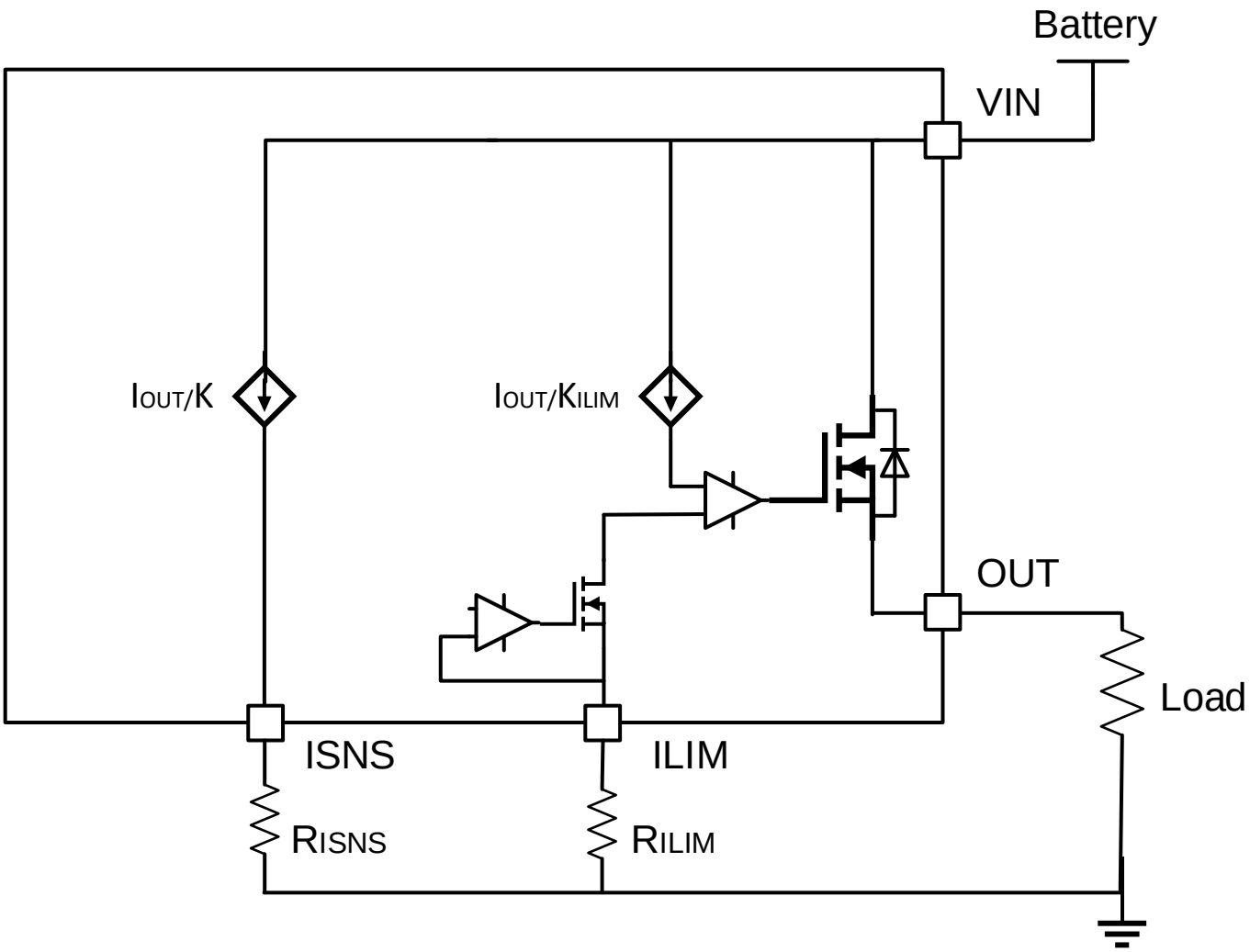

Figure 10-3. Current Sense and Current Limit Block Diagram

10.3 Programmable Current Limit

A high accuracy current limit allows higher reliability, which protects the power supply during short circuit or power up. Also, it can save system costs by reducing PCB traces, connector size, and the capacity of the preceding power stage.

Current limit protects the power path from overstressing. Current limit holds the current at the set value and pulls up the ISNS pin to V_{ISNS_h} as a diagnostic report. The two current-limit thresholds are:

• External programmable current limit -- An external resistor (R_{ILIM}) is used to generate the internal reference current which equals to V_{ILIM_th}/R_{ILIM}. When the sensed current (I_{OUT}/K_{ILIM}) exceeds V_{ILIM_th}/R_{ILIM}, a closed loop steps in to regulate the power FET Vgs. When the closed loop is set up, the current is clamped at the set value, V_{ILIM_th}/R_{ILIM}.

• Internal current limit -- The internal current limit is fixed and typically 10 A. Connecting the ILIM pin directly to the device GND will active the internal current limit.

Both the internal current limit (I_{LIM_int}) and external programmable current limit (I_{LIM_ext}) are always active when VIN is powered and EN is high. The lower one of the I_{LIM_int} and the I_{LIM_ext} is applied as the actual current limit.

When a GND network is used (1kΩ resistor in parallel with diode), the ILIM pin must be connected with the device GND. Calculate R_{ILIM} with Equation 2.

$$I_{ILIM} = \frac{V_{ILIM\_th}}{R_{ILIM}} = \frac{I_{OUT}}{K_{ILIM}} \rightarrow R_{ILIM} = \frac{V_{ILIM\_th} \times K_{ILIM}}{I_{OUT}} \quad (2)$$

For better protection from a hard short to GND condition, a fast-trip comparator is used to turn off the power FET, before the current limit closed loop is set up. The fast-trip comparator response time is around 1 µs. With this fast