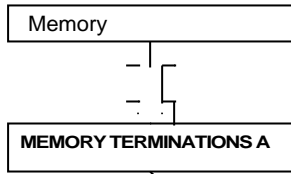
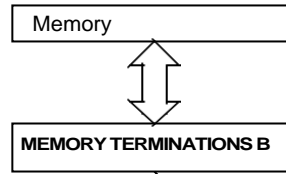


**MEMORY CHANNEL A**

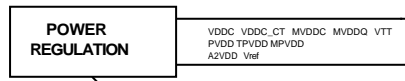
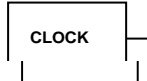


**MEMORY CHANNEL B**



MA[14..0] MDA[63..0] QSA[7..0] CS0A# DMA[0..7]  
 CASA# RASA# WEA# CKEA CLKA01 CLKA01#

MB[14..0] MDB[63..0] OSB[7..0] CS0B# DQMB[0..7]  
 CASB# RASB# WEA/B# CKEB/D CLKB01 CLKB01#



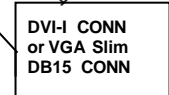
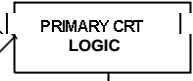
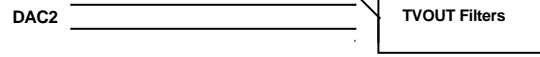
+3.3V\_BUS +5V\_BUS +12V\_BUS +VDDQ\_BUS  
 AD31..0 CBE3..0 CPUCLK STOP# PAR REQ#  
 IRDY# GNT# TRDY# DEVSEL# RESET#  
 FRAME# CLK INTR WBF# DBI\_HI DBI\_LO  
 AGPREF SBA[7..0] ST2..0 SB\_STB SB\_STB#  
 AD\_STB1 AD\_STB1# AD\_STB0 AD\_STB0# RBF#

MEM A MEM B

ROM

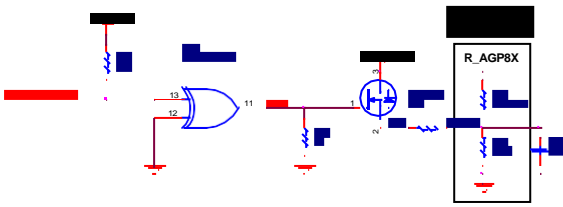
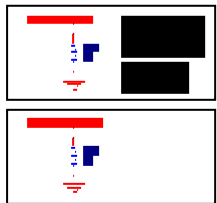
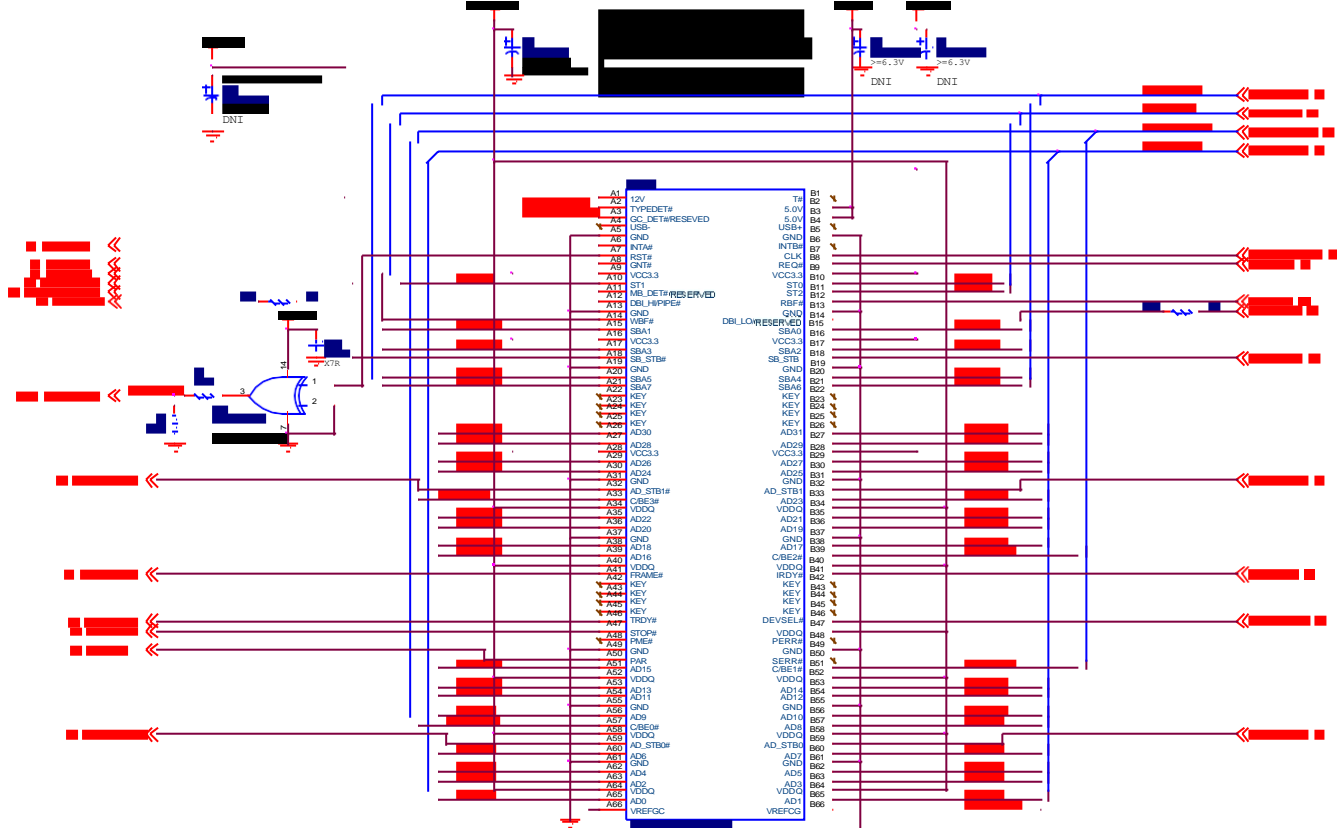
RV280

AGP

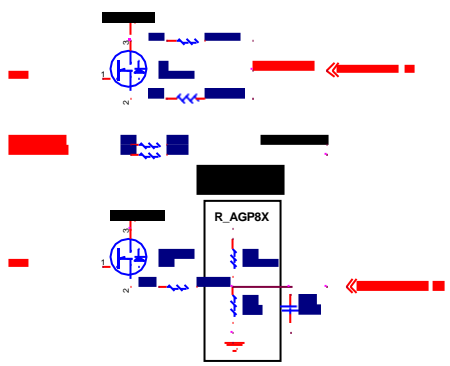


		<b>MICRO-STAR</b>	
Title: <b>BLOCK DIAGRAM</b>			
Size	Document Number	MS-8913	
Date:	Thursday, January 23, 2003	Sheet	2 of 16

The following grounds should be routed back to their respective regulators and then tied directly to the ground plane with one via: GND\_PVSS, GND\_MPVSS, GND\_TPVSS, and GND\_A2VSSN. The other ground pins (GND\_AVSSN, GND\_A2VSSQ, GND\_RSET, GND\_R2SET) should be tied to the ground plane directly through one via as close to the pins as possible without connecting to anything else. If space is an issue it is possible to use one via for two adjacent pins.



UNIVERSAL VREFGC CIRCUIT (2X, 4X, 8X)



MICRO-STAR  
 AGP AGP Bus 8X  
 MS-8913

(3) AGP\_AD[31:0] >> AGP\_AD[31:0]

GPIO[13:0] << GPIO[13:0] (9,10)

Part 1 of 5

AGP_AD0	K27
AGP_AD1	L26
AGP_AD2	L26
AGP_AD3	L27
AGP_AD4	M25
AGP_AD5	M26
AGP_AD6	N26
AGP_AD7	N25
AGP_AD8	R26
AGP_AD9	R25
AGP_AD10	T26
AGP_AD11	T25
AGP_AD12	U26
AGP_AD13	U25
AGP_AD14	U27
AGP_AD15	V26
AGP_AD16	M25
AGP_AD17	N29
AGP_AD18	N28
AGP_AD19	P29
AGP_AD20	P28
AGP_AD21	R29
AGP_AD22	R28
AGP_AD23	T28
AGP_AD24	V29
AGP_AD25	V28
AGP_AD26	W29
AGP_AD27	W28
AGP_AD28	Y28
AGP_AD29	Y28
AGP_AD30	AA29
AGP_AD31	AA28

GPIO0	AJ5
GPIO1	AJ4
GPIO2	AJ4
GPIO3	AJ4
GPIO4	AJ4
GPIO5	AJ4
GPIO6	AJ4
GPIO7	AJ3
GPIO8	AH3
GPIO9	AG3
GPIO10	AF3
GPIO11	AJ2
GPIO12	AG2
GPIO13	AG2
GPIO14	AF2
GPIO15	AG15
GPIO16	AG16
ROMCS#	AF15
DVOMCODE	AF15
ZV_LCDDATA0	AE8
ZV_LCDDATA1	AE6
ZV_LCDDATA2	AE7
ZV_LCDDATA3	AG6
ZV_LCDDATA4	AF7
ZV_LCDDATA5	AG8
ZV_LCDDATA6	AF8
ZV_LCDDATA7	AE9
ZV_LCDDATA8	AF9
ZV_LCDDATA9	AG9
ZV_LCDDATA10	AK7
ZV_LCDDATA11	AJ7
ZV_LCDDATA12	AH8
ZV_LCDDATA13	AJ8
ZV_LCDDATA14	AH8
ZV_LCDDATA15	AJ9
ZV_LCDDATA16	AK9
ZV_LCDDATA17	AH10
ZV_LCDDATA18	AK10
ZV_LCDDATA19	AJ10
ZV_LCDDATA20	AH11
ZV_LCDDATA21	AJ11
ZV_LCDDATA22	AH11
ZV_LCDDATA23	AH11
TL0	AK8
TL1	AJ8
TL2	AH8
TL3	AH7

RSET	499R	THE VALUES OF RSET AND R2SET SHOWN IN THE TABLE MAY BE APPROXIMATE VALUES ONLY (SUITABLE FOR PROTOTYPE) BEFORE GOING INTO PRODUCTION, CONTACT YOUR AT&T REPRESENTATIVE FOR THE RSET/R2SET VALUES QUALIFIED FOR MASS PRODUCTION.
R2SET	715R	

(3) AGP\_CBE[3:0] >> AGP\_CBE[3:0]

(3) AGP\_AGPICLK >> R36

(3,15) AGP\_RESET#

(3) AGP\_RE0#

(3) AGP\_GNT#

(3) AGP\_PAR

(3) AGP\_STOP#

(3) AGP\_DEVSEL#

(3) AGP\_TRDY#

(3) AGP\_IRDY#

(3) AGP\_FRAME#

(3) AGP\_INTR#

(3) AGP\_WBF#

(3) AGP\_RBF#

(3) AGP\_AD\_STB0

(3) AGP\_AD\_STB1

(3) AGP\_SB\_STB

(3) AGP\_SBA[7:0] >> AGP\_SBA[7:0]

(3) AGP\_ST[2:0] >> AGP\_ST[2:0]

(3) AGP\_AGPREFCG >> C20

(3) AGP\_AGPTEST >> C20

(15) A\_R\_C\_DAC2

(15) A\_G\_Y\_DAC2

(15) A\_B\_COMP\_DAC2

To update: XTAL to 10ppm

(15) RT\_XTALOUT >> R1265

XTALOUT >> R1269

(15) RT\_XTALIN >> R1271

EXT TMSDS / GPIO / ROM

AGP_CBE[3:0]	Y25
AGP_CBE[2:0]	M29
AGP_CBE[3]	T29
PCICLK	AF29
RSTB	AE29
RC2B	AG28
GNTb	AG28
PAR	AG28
STOP#	K29
DEVSELb	K29
TRDY#	L29
IRDY#	L29
FRAME#	L28
INTAB	AF28
WBF#	AF27
NC19	AK19
NC18	AK18
NC17	AK17
NC16	AK16
AD_STBF0	Y26
AD_STBF1	Y26
SB_STBF	Y26
SB_A0	AE27
SB_A1	AE26
SB_A2	AC25
SB_A3	AC26
SB_A4	AC25
SB_A5	AC26
SB_A6	Y26
SB_A7	Y26
AD28	AD28
ST0	ST0
ST1	ST1
ST2	ST2
SB_STB5	AE25
AD_STB50	U26
AD_STB51	M29
AGPREF	H28
AGPTEST	AG27
AGPRX_DETb	AE28
DBI_HI	AE29
DBI_LO	AE29
R2SET	AJ21
C_R	AJ22
Y_G	AK21
COMP_B	AG25
HSYNC	AG25
VS2SYNC	AG25
CRT2DDCLK	AF23
CRT2DDCDAT	AG24
NC34	AG29
NC33	AG29
XTALIN	AJ28
XTALOUT	AJ29
TESTEN	AH26
STEREOSYNC	AJ27
STEREOSYNC	AG

PC/AGP

VIDDV00	AE8
VIDDV01	AE7
VIDDV02	AG6
VIDDV03	AF7
VIDDV04	AG8
VIDDV05	AF8
VIDDV06	AE9
VIDDV07	AF9
DC_Strap1	AK7
DC_Strap2	AJ7
DC_Strap3	AJ8
DC_Strap4	AH8
LCCDATA16	AJ9
LCCDATA17	AK9
PALNTSC	AH10
DC_Strap5	AJ10
LCCDATA20/VHADO	AH11
VHAD1	AH11
VPHCTL	AH11
CLK_VIPCLK	AH11
CLK_VIDCLK	AH7

AGP2X

NC35	AE15
NC27	AE16
NC26	AE16
NC28	AG16
NC28	AG16
NC37	AH15
NC29	AH15
NC30	AH15
NC31	AF17
NC38	AG17
NC30	AJ17
NC22	AH16
NC13	AK18
NC23	AJ18
NC14	AG18
NC24	AH18
NC15	AJ16
NC26	AK16
NC17	AH20
NC25	AH20
NC16	AF11
NC1	AF11
NC3	AE12

AGP4X/8X

DPLUS	AE10
DMINUS	AE11
TX0M	AH13
TX0P	AJ13
TX1M	AH14
TX1P	AJ14
TX2M	AH15
TX2P	AJ15
TX3M	AK15
TX3P	AK15
TXCM	AK12
TXCP	AK13
DVIDDCCLK	AF13
DVIDCCDATA	AE13
HPD	AF12
HPD	AF12
A_R_DAC1	AK25
A_G_DAC1	AJ25
A_S_DAC1	AK24
A_HSYNC_DAC1	AH28
A_VSYNC_DAC1	AH27
CRT1DDCCDATA	AG26
CRT1DDCCCLK	AF26

TMDS

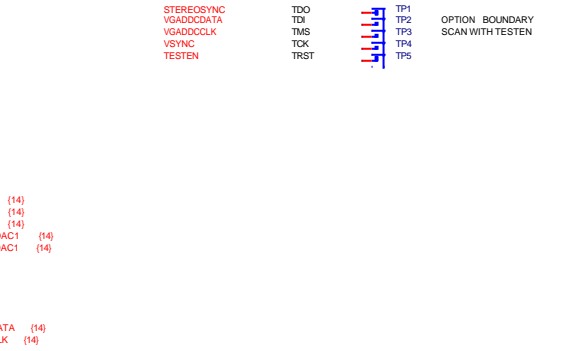
TX0M	AH13
TX0P	AJ13
TX1M	AH14
TX1P	AJ14
TX2M	AH15
TX2P	AJ15
TX3M	AK15
TX3P	AK15
TXCM	AK12
TXCP	AK13
DVIDDCCLK	AF13
DVIDCCDATA	AE13
HPD	AF12
HPD	AF12
A_R_DAC1	AK25
A_G_DAC1	AJ25
A_S_DAC1	AK24
A_HSYNC_DAC1	AH28
A_VSYNC_DAC1	AH27
CRT1DDCCDATA	AG26
CRT1DDCCCLK	AF26

DAC2

A_R_DAC1	AK25
A_G_DAC1	AJ25
A_S_DAC1	AK24
A_HSYNC_DAC1	AH28
A_VSYNC_DAC1	AH27

DAC1

A_R_DAC1	AK25
A_G_DAC1	AJ25
A_S_DAC1	AK24
A_HSYNC_DAC1	AH28
A_VSYNC_DAC1	AH27



Some Part Ref's updated to 988 brd

MICRO-STAR

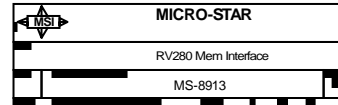
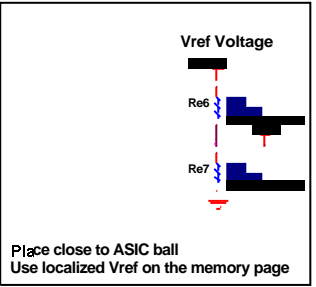
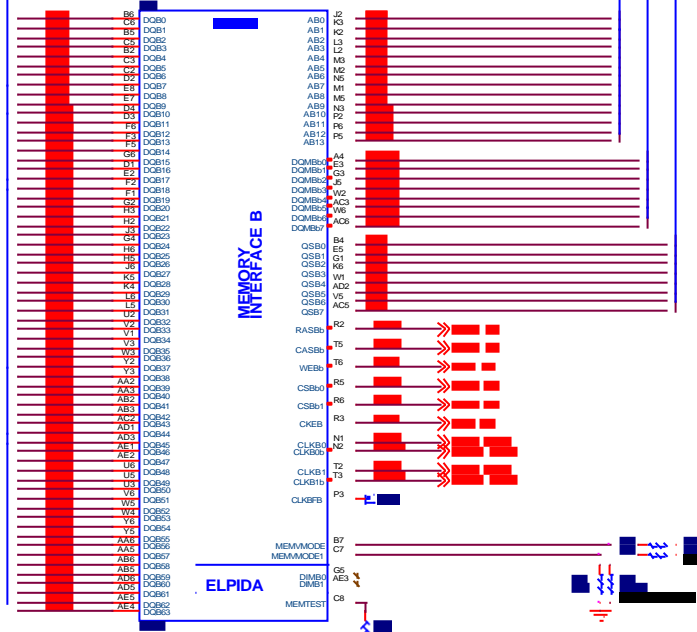
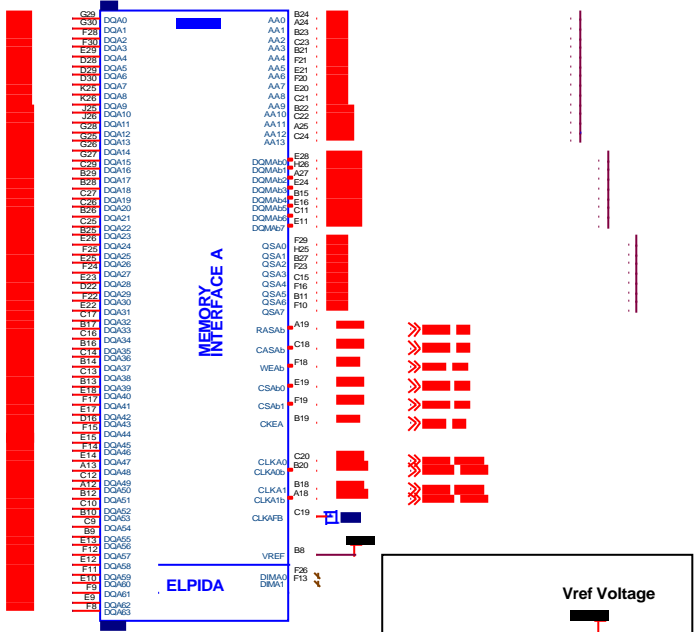
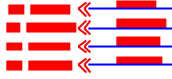
AGP RV280 Core

MS-8913

Monday, February 10, 2003

MEMORY CHANNEL A

MEMORY CHANNEL B



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