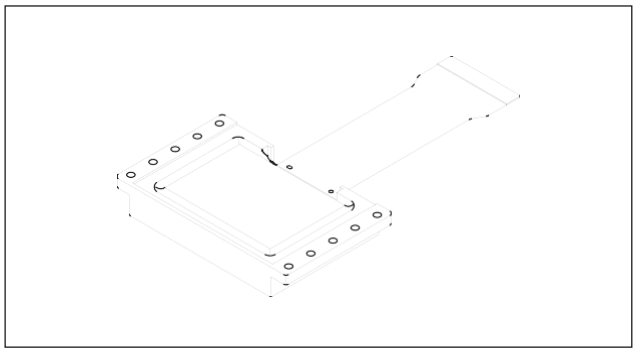
SONY

LCX011AM

3.6cm (1.43-inch) LCD Panel (with microlens)



Description

The LCX011AM is a 3.6cm diagonal active matrix TFT-LCD panel addressed by polycrystalline silicon super thin film transistors with built-in peripheral driving circuit. This panel allows full-color representation without color filters through the use of a microlens.

This panel provides a wide aspect ratio of 16:9, such as those represented in HD. The built-in side- black function also allows an aspect ratio of 4:3 in the NTSC/PAL mode.

This panel has a polysilicon TFT high-speed scanner and built-in function to display images up/down and/or right/left inverse. The built-in 5V interface circuit leads to lower voltage of timing and control signals.

Features

- The number of active dots: 768,000 (1.43-inch; 3.6cm in diagonal)
- Horizontal resolution: 600TV lines
- Effective aperture ratio: 70% (reference value)
- High contrast ratio with normally white mode: 200 (typ.)
- Built-in H and V drivers (built-in input level conversion circuit, 5V driving possible)
- NTSC/NTSC-WIDE/HD (band: 20MHz) mode selectable
  (PAL/PAL-WIDE mode also available through conversion of scanned dot numbers by an external IC)
- Up/down and/or right/left inverse display function
- Side-black function
- 16:9 and 4:3 aspect-ratio switching function

Element Structure

- Dots
  16:9 display: 1599.5 (H) × 480 (V) = 767,760
  4:3 display: 1199.5 (H) × 480 (V) = 575,760

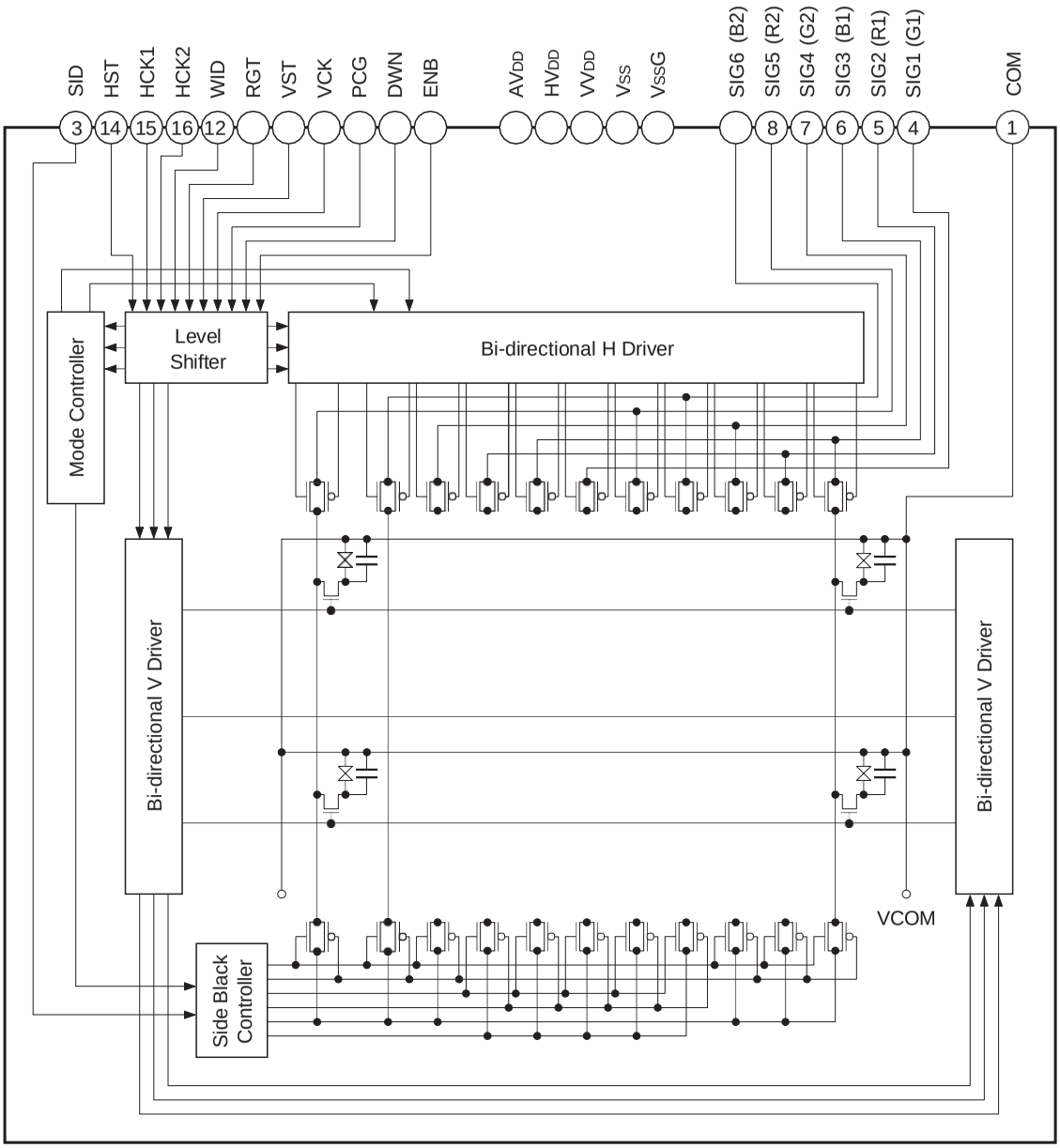
- Built-in peripheral driver using polycrystalline silicon super thin film transistors.

Applications

Liquid crystal projectors, etc.

E96919A94-PS

Block Diagram



Absolute Maximum Ratings (V_{SS} = 0 V)

• H driver supply voltage	HV_{DD}	–1.0 to +20	V
• V driver supply voltage	VV_{DD}	–1.0 to +20	V
• Analog block drive supply voltage	AV_{DD}	–1.0 to +20	V
• Common pad voltage	COM	–1.0 to +17	V
• H shift register input pin voltage	HST, HCK1, HCK2 RGT, WID	–1.0 to +17	V
• V shift register input pin voltage	VST, VCK, PCG ENB, DWN	–1.0 to +17	V
• Video signal input pin voltage	SIG1, SIG2, SIG3, SIG4 SIG5, SIG6, SID	–1.0 to +15	V
• Operating temperature	Topr	–10 to +70	°C
• Storage temperature	Tstg	–30 to +85	°C

Operating Conditions (V_{SS} = 0V)

• Supply voltage

HV_{DD}	13.5 ± 0.3	V
VV_{DD}	13.5 ± 0.3	V
AV_{DD}	15.5 ± 0.3	V

• Input pulse voltage (Vp-p of all input pins except video signal and side black signal input pins)

Vin	5.0 ± 0.5	V

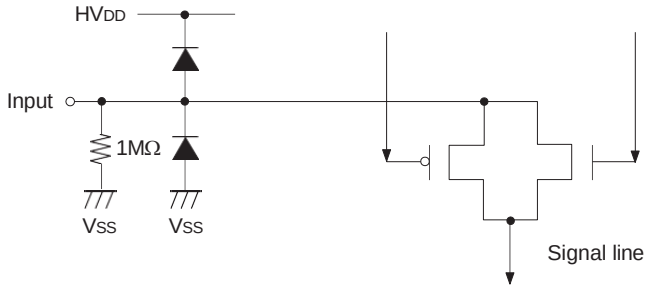
Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	COM	Common voltage of panel	13	RGT	Drive direction pulse for H shift register (H: normal, L: reverse)
2	$V_{SS}G$	Analog block GND	14	HST	Start pulse for H shift register drive
3	SID	Side black signal for 4:3 display	15	HCK1	Clock pulse for H shift register drive
4	SIG1 (G1)	Video signal 1 (G) to panel	16	HCK2	Clock pulse for H shift register drive
5	SIG2 (R1)	Video signal 2 (R) to panel	17	V_{SS}	GND (H, V drivers)
6	SIG3 (B1)	Video signal 3 (B) to panel	18	ENB	Enable pulse for gate selection
7	SIG4 (G2)	Video signal 4 (G) to panel	19	VCK	Clock pulse for V shift register drive
8	SIG5 (R2)	Video signal 5 (R) to panel	20	VST	Start pulse for V shift register drive
9	SIG6 (B2)	Video signal 6 (B) to panel	21	DWN	Drive direction pulse for V shift register (H: normal, L: reverse)
10	AV_{DD}	Analog block power supply	22	PCG	Improvement pulse (2) for uniformity
11	HV_{DD}	Power supply for H driver	23	VV_{DD}	Power supply for V driver
12	WID	Aspect-ratio switching (H: 16:9, L: 4:3)	24	TEST	Test; Open

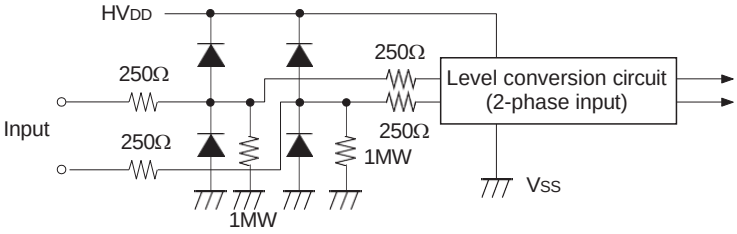
Input Equivalent Circuit

To prevent static charges, protective diodes are provided for each pin except the power supply. In addition, protective resistors are added to all pins except video signal input. All pins are connected to Vss with a high resistance of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (The resistor value: typ.)

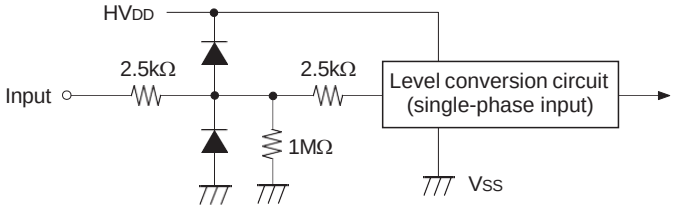
(1) SIG1, SIG2, SIG3, SIG4, SIG5, SIG6, SID



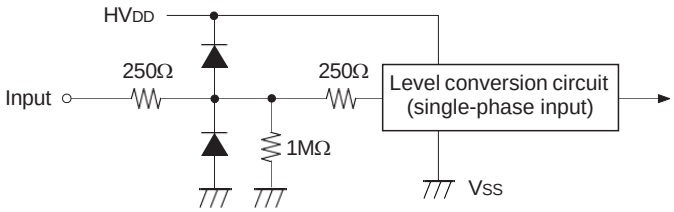
(2) HCK1, HCK2



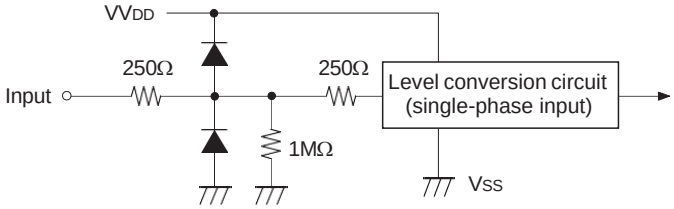
(3) RGT, WID



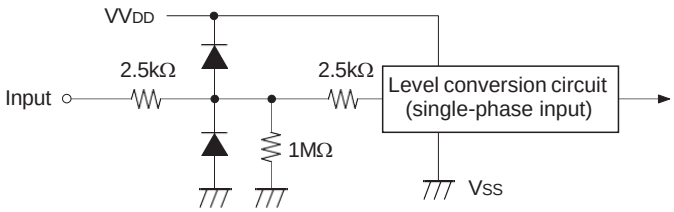
(4) HST



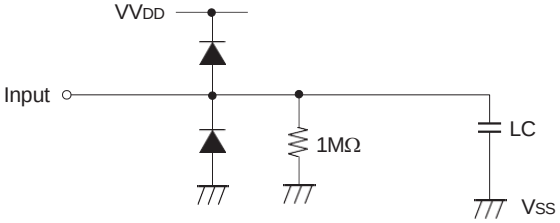
(5) PCG, VCK



(6) VST, ENB, DWN



(7) COM



Input Signals

1. Input signal voltage conditions

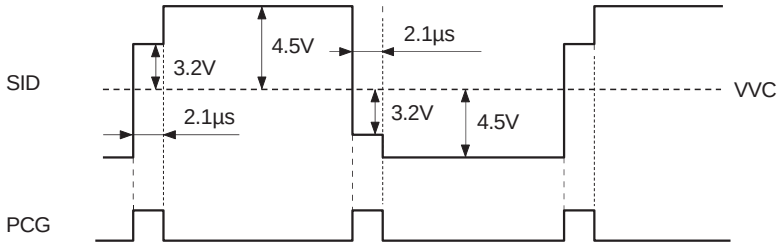
(Vss = 0V)

Item		Symbol	Min.	Typ.	Max.	Unit
H driver input voltage WID, RGT, HST, HCK1, HCK2	(Low)	VHIL	–0.5	0.0	0.3	V
	(High)	VHIH	4.5	5.0	5.5	V
V driver input voltage ENB, VCK, PCG, VST, DWN	(Low)	VVIL	–0.5	0.0	0.3	V
	(High)	VVIH	4.5	5.0	5.5	V
Video signal center voltage		VVC	6.8	7.0	7.2	V
Video signal input range*1 (SIG1 to 6)		Vsig	VVC – 4.5	—	VVC + 4.5	V
Common voltage of panel*2		Vcom	VVC – 0.3	VVC – 0.2	VVC – 0.1	V
Side black signal for 4:3 display*3 (SID) input voltage		Vsid	VVC ± 4.4 (VVC ± 3.1)	VVC ± 4.5 (VVC ± 3.2)	VVC ± 4.6 (VVC ± 3.3)	V

*1 Video input signal shall be symmetrical to VVC.

*2 Common voltage of the panel shall be adjusted to VVC – 0.2V.

*3 The side black signal for 4:3 display shall be input at the timing shown in the figure below. Also, the interval between the SID rise and fall shall be kept to 800ns or less.



Level Conversion Circuit

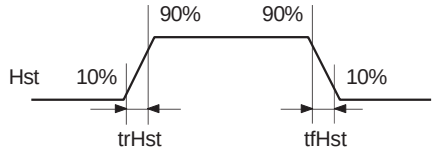
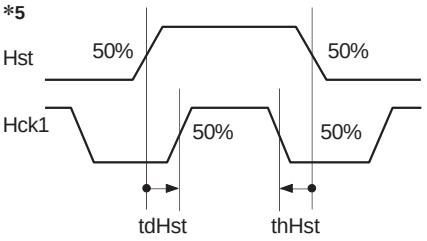
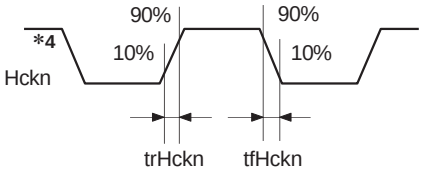
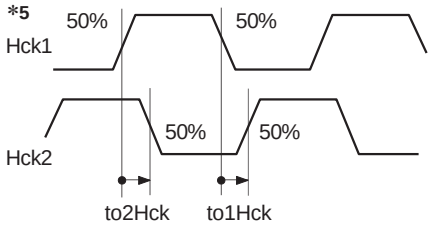
The LCX011AM has a built-in level conversion circuit in the clock input unit on the panel. The input signal level increases to HV_{DD} or VV_{DD}. The V_{CC} of external ICs are applicable to 5 ± 0.5V.

2. Clock timing conditions (16:9 display mode) (Ta = 25°C) (fHCKn = 5.6MHz, fVCK = 15.7kHz)

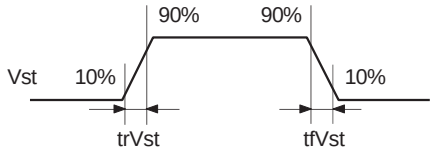
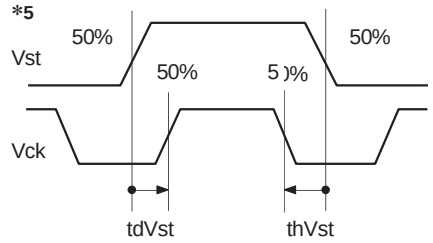
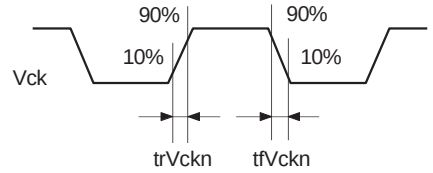
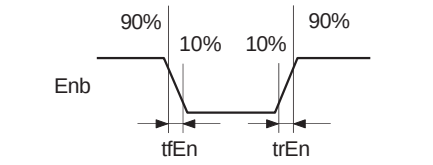
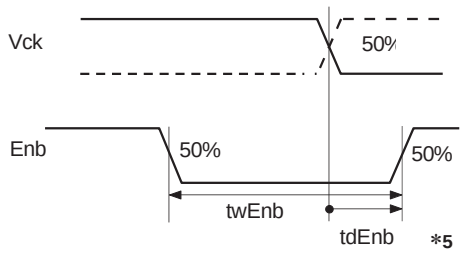
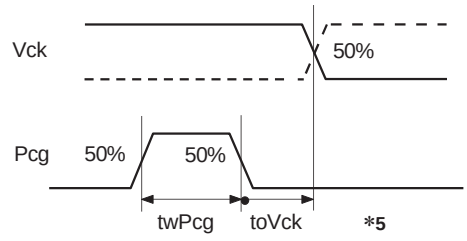
	Item	Symbol	Min.	Typ.	Max.	Unit
HST	Hst rise time	trHst	—	—	30	ns
	Hst fall time	tfHst	—	—	30	
	Hst data set-up time	tdHst	74	89	104	
	Hst data hold time	thHst	–15	0	15	
HCK	Hckn*4 rise time	trHckn	—	—	30	
	Hckn*4 fall time	tfHckn	—	—	30	
	Hck1 fall to Hck2 rise time	to1Hck	–15	0	15	
	Hck1 rise to Hck2 fall time	to2Hck	–15	0	15	
VST	Vst rise time	trVst	—	—	100	
	Vst fall time	tfVst	—	—	100	
	Vst data set-up time	tdVst	5	15	25	µs
	Vst data hold time	thVst	5	15	25	
VCK	Vck rise time	trVck	—	—	100	ns
	Vck fall time	tfVck	—	—	100	
ENB	Enb rise time	trEnb	—	—	100	
	Enb fall time	tfEnb	—	—	100	
	Vck rise/fall to Enb rise time	tdEnb	350	400	450	
	Enb pulse width	twEnb	3450	3500	3550	
PCG	Pcg rise time	trPcg	—	—	20	
	Pcg fall time	tfPcg	—	—	20	
	Pcg fall to Vck rise/fall time	toVck	–50	0	50	
	Pcg pulse width	twPcg	2050	2100	2150	

*4 Hckn means Hck1 and Hck2.

<Horizontal Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
HST	Hst rise time	trHst		• Hckn*4 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst fall time	tfHst		
	Hst data set-up time	tdHst		• Hckn*4 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst data hold time	thHst		
HCK	Hckn*4 rise time	trHckn		• Hckn*4 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hckn*4 fall time	tfHckn		
	Hck1 fall to Hck2 rise time	to1Hck		
	Hck1 rise to Hck2 fall time	to2Hck		

<Vertical Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
VST	Vst rise time	trVst		
	Vst fall time	tfVst		
	Vst data set-up time	tdVst		
	Vst data hold time	thVst		
VCK	Vck rise time	trVck		
	Vck fall time	tfVck		
ENB	End rise time	trEnb		
	End fall time	tfEnb		
	Vck rise/fall to Enb rise time	tdEnb		
	Enb pulse width	twEnb		
PCG	Pcg rise time	trPcg		
	Pcg fall time	tfPcg		
	Pcg fall to Vck rise/fall time	toVck		
	Pcg pulse width	twPcg		

*5 Definitions: The right-pointing arrow (•→) means +.
The left-pointing arrow (←•) means –.
The black dot at an arrow (•) indicates the start of measurement.

Electrical Characteristics (Ta = 25°C, HV_{DD} = 13.5V, VV_{DD} = 13.5V, AV_{DD} = 15.5V)

1. Horizontal drivers

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input pin capacitance HCKn	CHckn	—	12	17	pF	
HST	CHst	—	12	17	pF	
Input pin current HCK1		–500	–100	—	µA	HCK1 = GND
HCK2		–1000	–350	—	µA	HCK2 = GND
HST		–500	–150	—	µA	HST = GND
WID, RGT		–150	–30	—	µA	WID, RGT = GND
Video signal input pin capacitance	Csig	—	250	—	pF	
Current consumption	IH	—	5.5	10	mA	HCKn: HCK1, HCK2 (5.6MHz)

2. Vertical drivers

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input pin capacitance VCK	CVck	—	12	17	pF	
VST	CVst	—	12	17	pF	
Input pin current VCK		–500	–150	—	µA	VCK = GND
PCG, VST, ENB, DWN		–150	–30	—	µA	PCG, VST, EN, DWN = GND
Current consumption	IV	—	1.1	4	mA	VCK: (15.7kHz)

3. Analog block

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Current consumption	IA	—	2	4	mA	HCKn, HCK1, HCK2 (5.6MHz) VCK (15.7kHz)

4. Total power consumption of the panel

Item	Symbol	Min.	Typ.	Max.	Unit
Total power consumption of the panel (NTSC)	PWR	—	120	250	mW

5. Pin input resistance

Item	Symbol	Min.	Typ.	Max.	Unit
Pin-V_{SS} input resistance	Rpin	0.4	1	—	MΩ

6. Side signal input pin capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Side signal input pin capacitance	CSIDon	—	13	16	nF

Electro-optical Characteristics (Ta = 25°C, NTSC mode)

Item			Symbol	Measure-ment method	Min.	Typ.	Max.	Unit
Contrast ratio		60°C	CR60	1	130	200	—	—
Effective aperture ratio		60°C	Teff	2	60	70	—	%
V-T characteristics	V_{90}	25°C	RV_{90-25}	3	1.0	1.3	1.7	V
			GV_{90-25}		1.0	1.4	1.8	
			BV_{90-25}		1.1	1.5	1.9	
		60°C	RV_{90-60}		1.0	1.3	1.7	
			GV_{90-60}		1.0	1.4	1.8	
			BV_{90-60}		1.1	1.5	1.9	
	V_{50}	25°C	RV_{50-25}		1.3	1.6	1.9	
			GV_{50-25}		1.4	1.7	2.0	
			BV_{50-25}		1.5	1.8	2.1	
		60°C	RV_{50-60}		1.4	1.7	2.1	
			GV_{50-60}		1.4	1.7	2.1	
			BV_{50-60}		1.5	1.8	2.2	
	V_{10}	25°C	RV_{10-25}		1.7	2.1	2.6	
			GV_{10-25}		1.7	2.1	2.6	
			BV_{10-25}		1.8	2.2	2.7	
		60°C	RV_{10-60}		1.7	2.1	2.6	
			GV_{10-60}		1.8	2.2	2.7	
			BV_{10-60}		1.8	2.2	2.7	
Response time	ON time	0°C	ton0	4	—	30	80	ms
		25°C	ton25		—	12	40	
	OFF time	0°C	toff0		—	100	200	
		25°C	toff25		—	30	70	
Flicker		60°C	F	5	—	–65	–40	dB
Image retention time		25°C	YT60	6	—	—	0	s
Cross talk		25°C	CTK	7	—	—	5	%